Effect of Electrical Stress on GaN HEMTs

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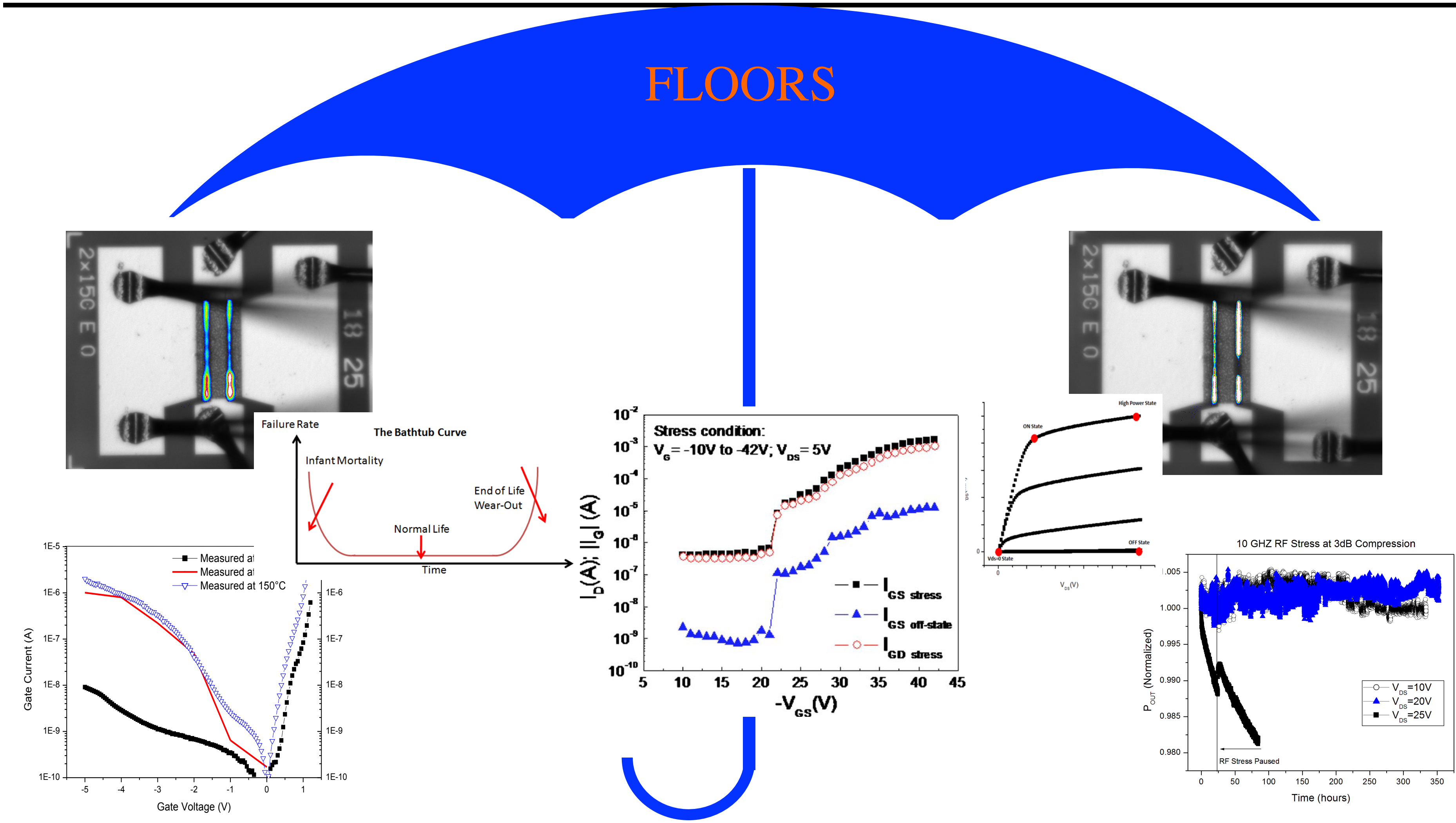
GATOR Engineering
UNIVERSITY OF FLORIDA

Overview

I. Introduction
II. DC Stress Results
  A. Field-Driven Degradation
  B. Trap Density
  C. Effect of Temperature
III. RF Stress Results
  A. Drain Bias Dependence
  B. Photoemission
IV. Conclusion

Electrical Characterization & Stress



t=0, As Built → t>0, Degradation

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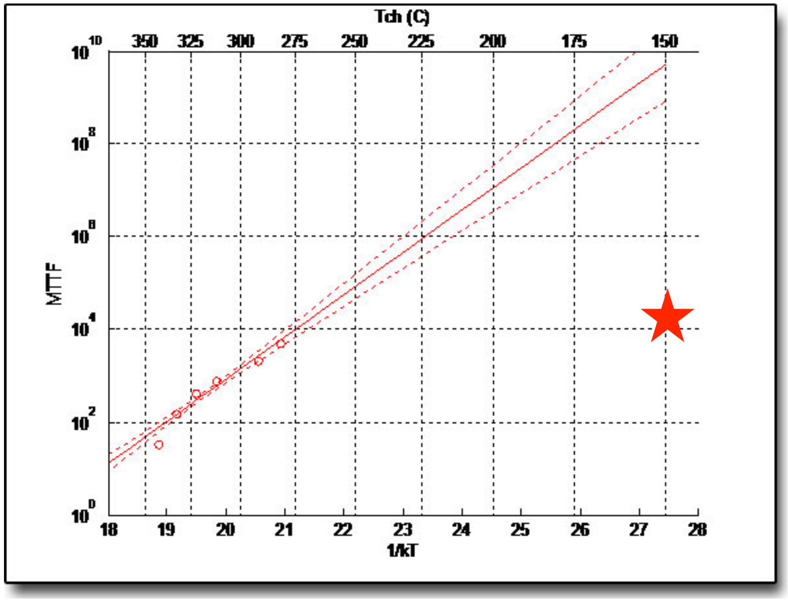
Introduction

- AlGaN/GaN HEMTs show exceptional promise for radar systems, high frequency & high power communications.
- MTTF > 10^6 hours at 200°C

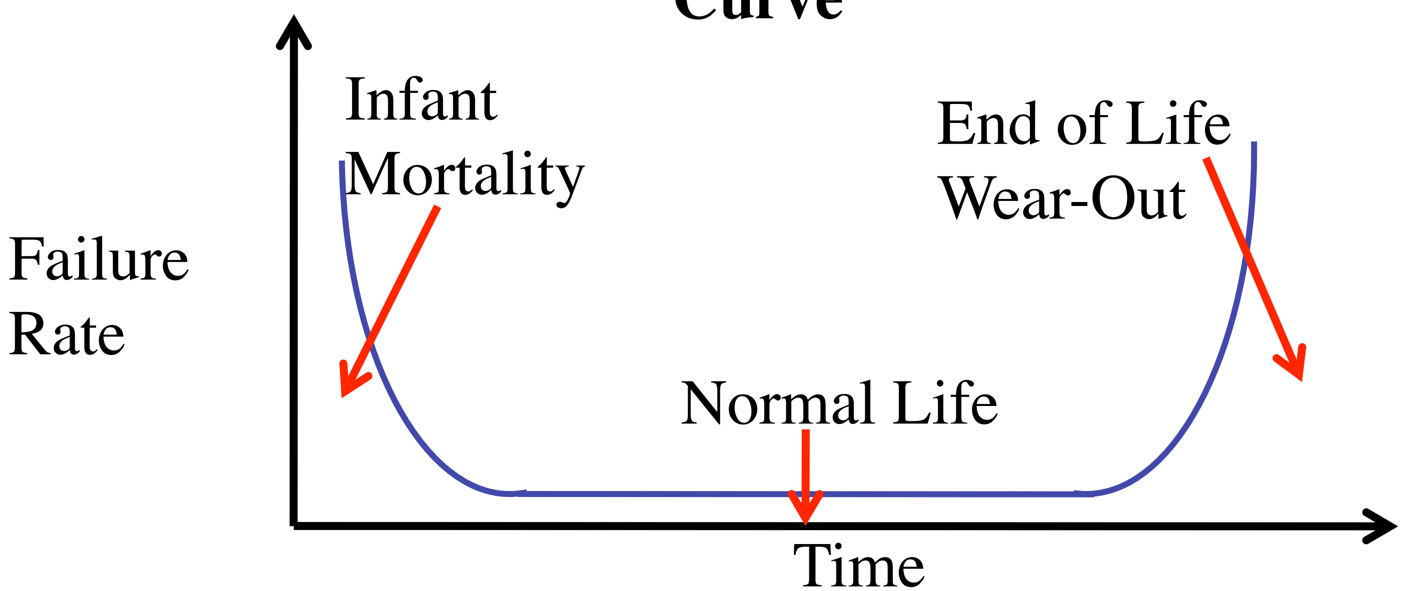
  > 10^7 hours at lower temperatures
- Fundamental mechanisms due to electrical degradation still unknown.



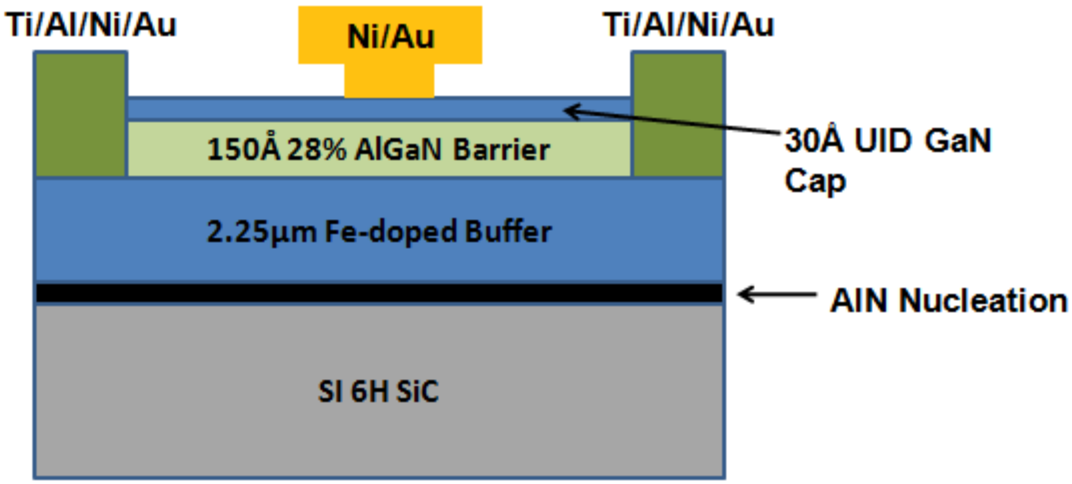
Motivation

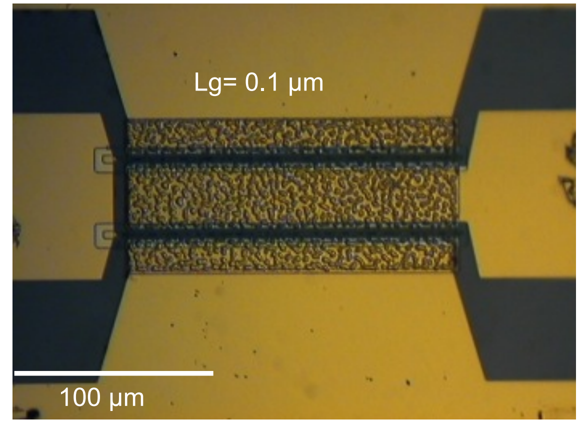
- Reduce early failures – Develop electrical characterization suite for prescreening
- Decrease random failures – Understand fundamental degradation mechanisms
- Increase device lifetime – Use simulations to optimize device design

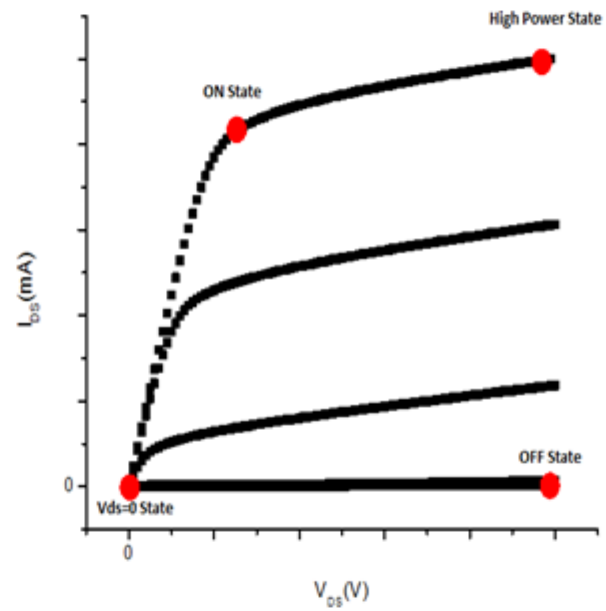
The Bathtub Curve



Device Structure







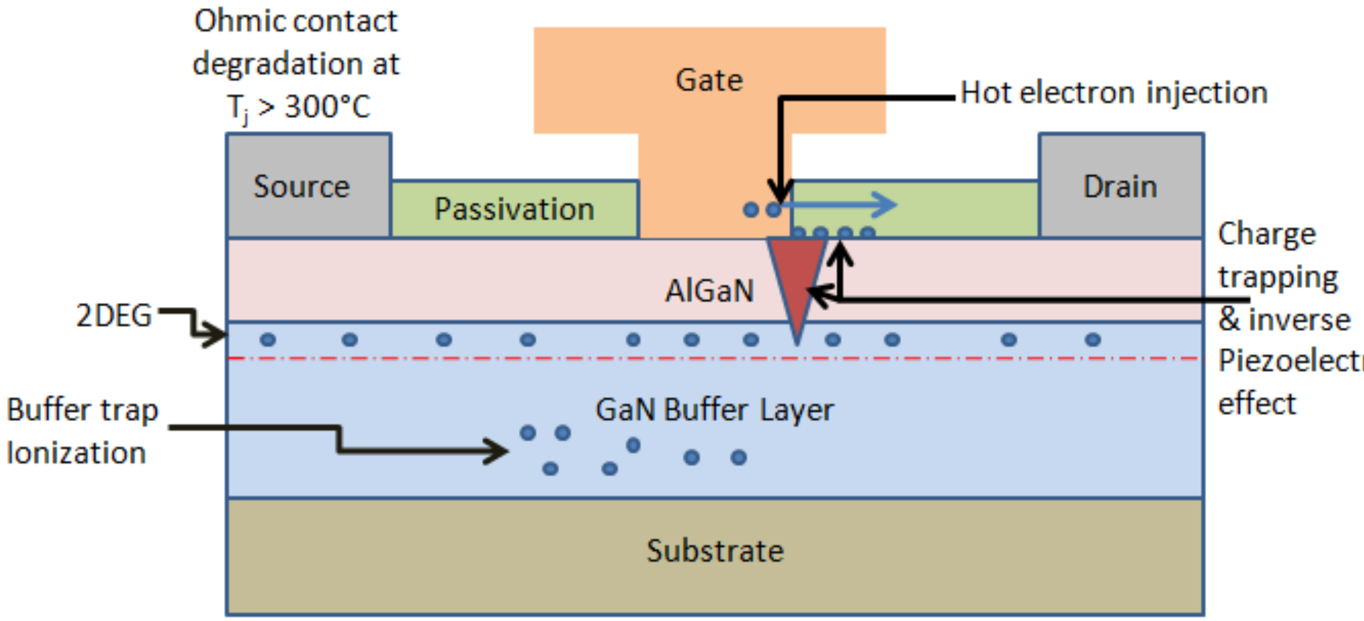
ICP mesa etch of ~1000Å

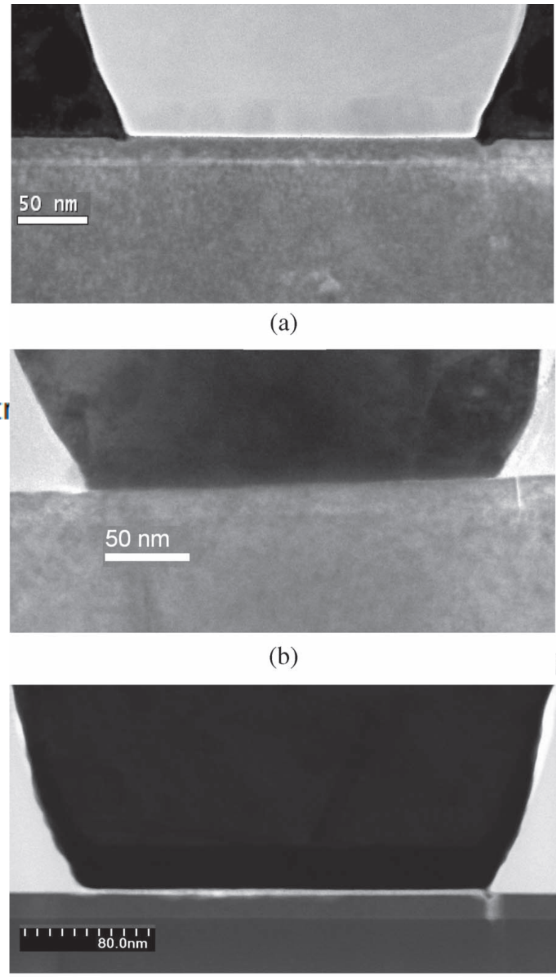
Ohmic contacts annealed at 850° C for 30 sec

Silicon nitride passivation

Gate length: 0.1μm to 1μm

GaN HEMT Degradation





(a)

(b)

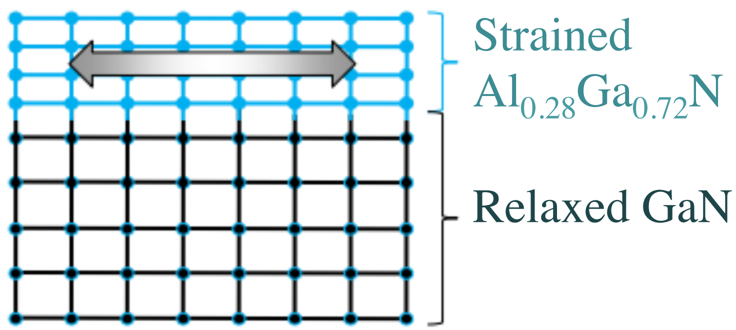
(c)

Degradation Mechanisms:
1) Hot Electrons
2) Contact Degradation
3) Inverse Piezoelectric Effect

J. A. del Alamo, C. V. Thompson, T. Palacios, DRIFT MURI, 2009.

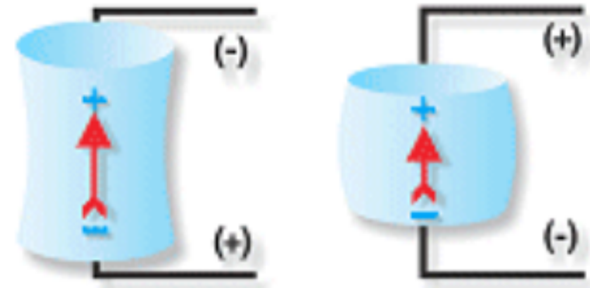
GaN HEMT Degradation (2)

Process Stressors
(Lattice Mismatch)

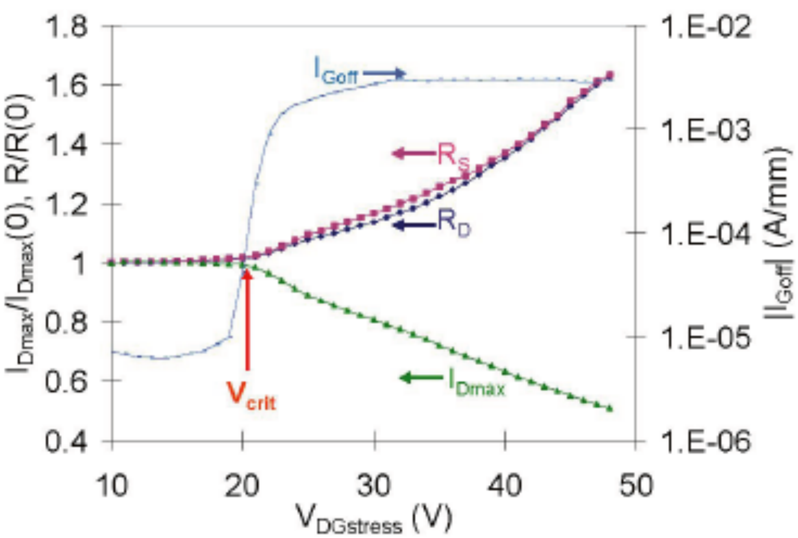


2.8 GPa Biaxial Tensile

Bias Stressors
(Inverse Piezoelectric Effect)



~500 MPa Biaxial Tensile
(V_{GS} = 30 V)



J. W. Joh, L. Xia, and J. A. del Alamo IEDM 2007

Hypothesis: Field-induced stress results in degradation.

Goal: To systematically investigate effect of electrical stress on gate degradation.

Courtesy Nishida's Group, MURI, 2011

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Stress Conditions – DC

I. V_{GS} step stressed from -10V to -42V in -1 V step at V_{DS}= 0V state; Source and drain grounded (Center gate, 2μm spacing)

II. V_{GS} step stressed from -5V to -42V for different value of V_{DS}. V_{DS}= 0V, 5V, 10V and 15V, respectively. (100nm center gate) (Off-state Stress)

III. V_{GS} step stressed from -10V to -42V with V_{DS} =5V.
- EL & PL

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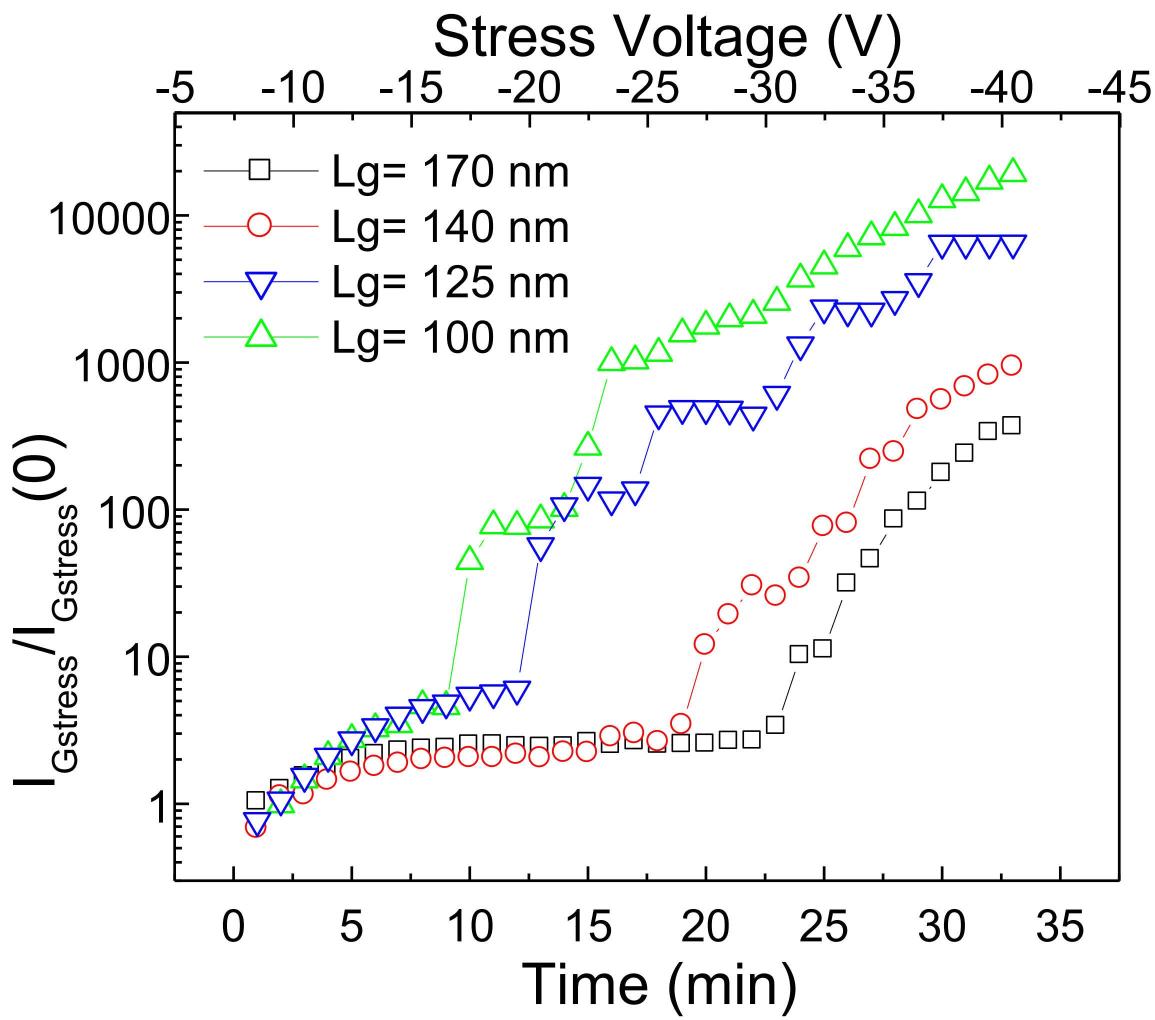
- EL & PL

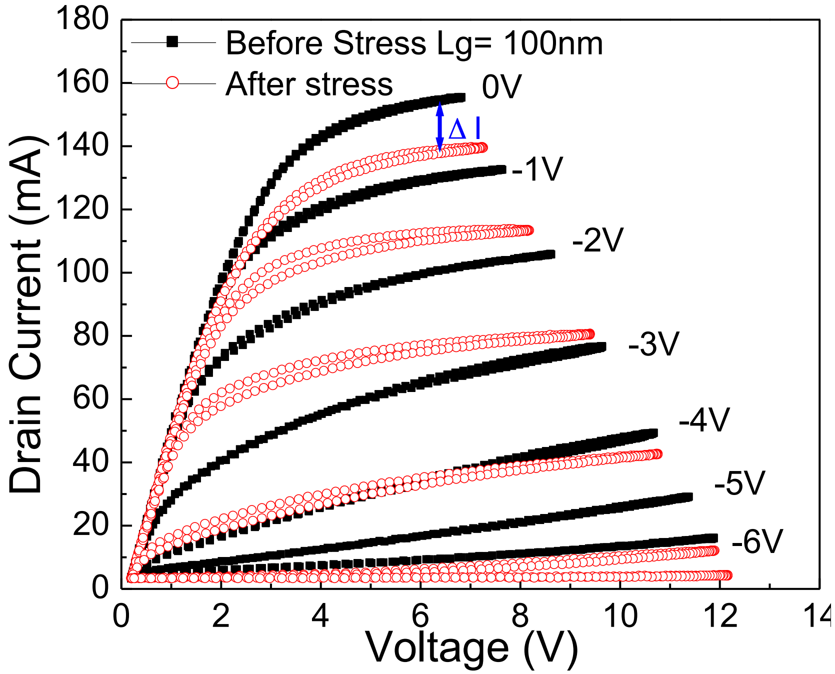
Field Driven Degradation

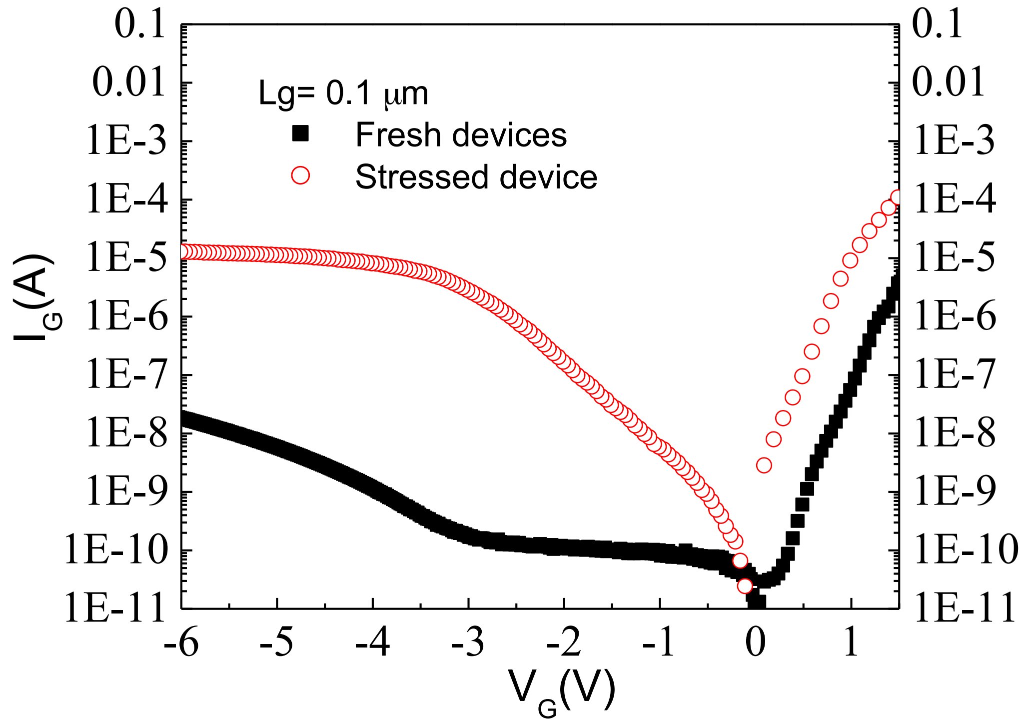


- Strong dependence of V_{CRI} on gate length
- Step-wise feature present on most devices

C.-Y. Chang, E. A. Douglas, *et al.*, *IEEE Trans Materials and Device Reliability* **11**, 1 (2011).

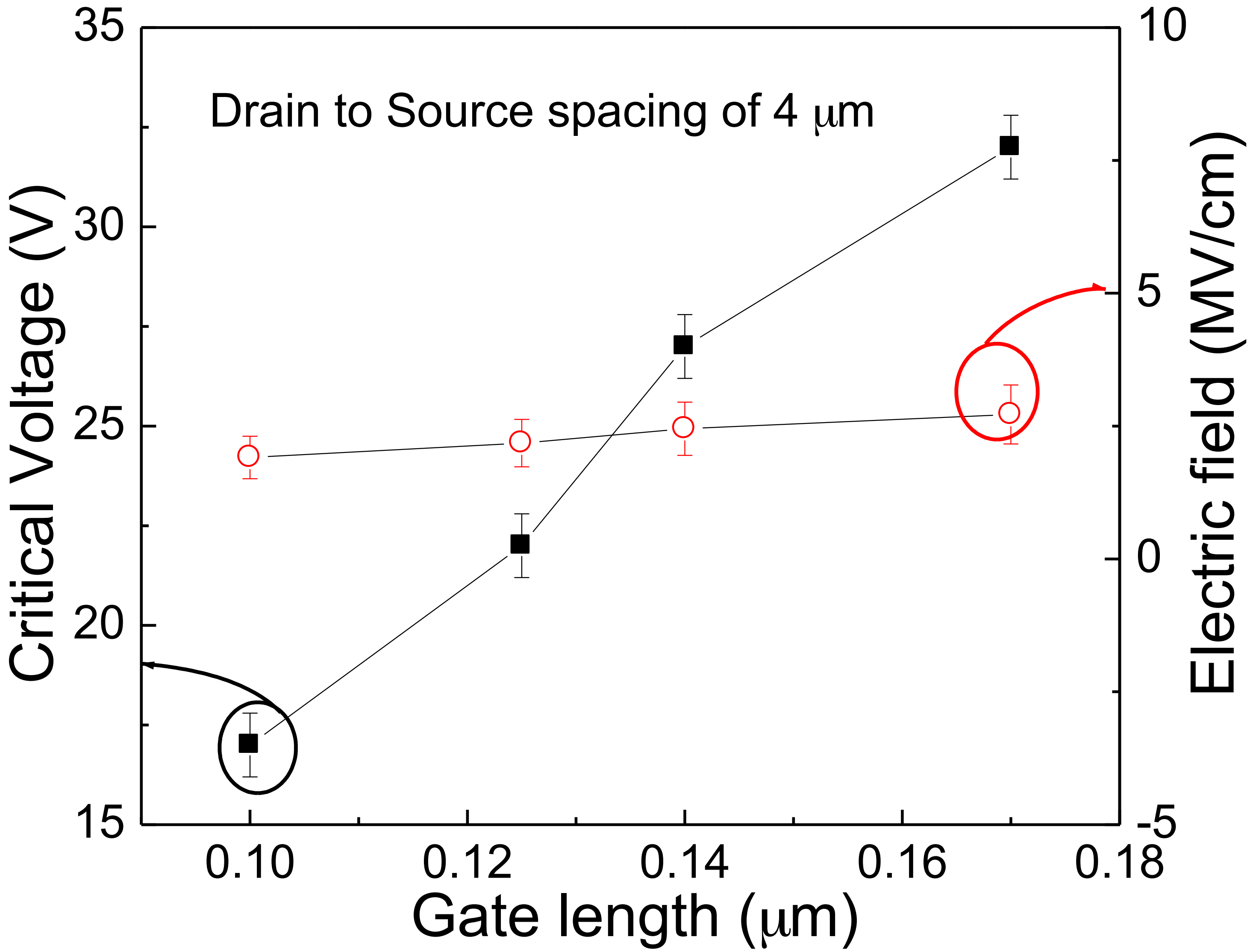
Field Driven Degradation (2)





- Minimal decrease in I_{DSS} (~ 10% - 20%)
- Large increase in I_{GS} (3 – 4 orders of magnitude)

Field Driven Degradation (3)



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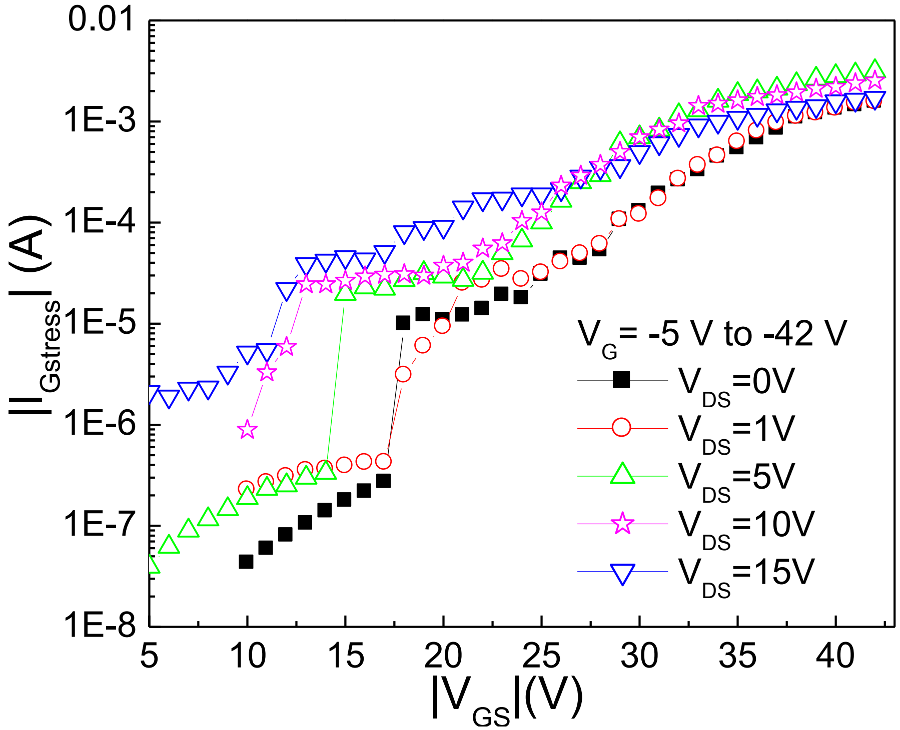
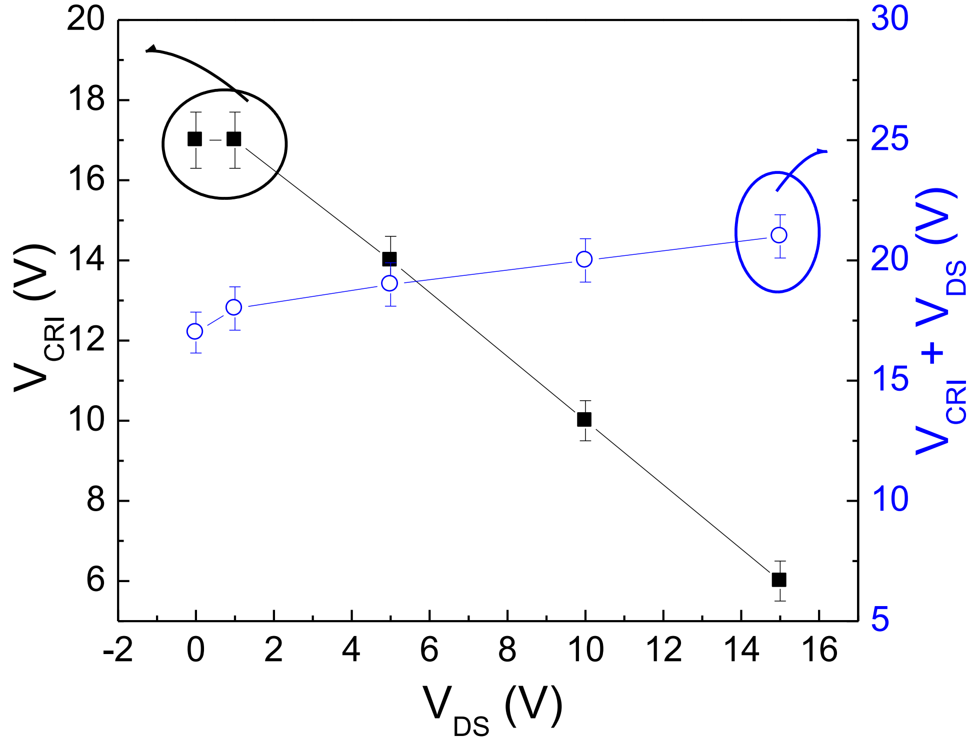
- EL & PL

Effect of Drain Bias



Change in stress gate current in step-stress experiments for different values of V_{DS}.



(Critical voltage + applied drain voltage) as a function of applied drain voltage

E. A. Douglas, *et al.*, *Microelectronics Reliability* **51**, 2 (2011).

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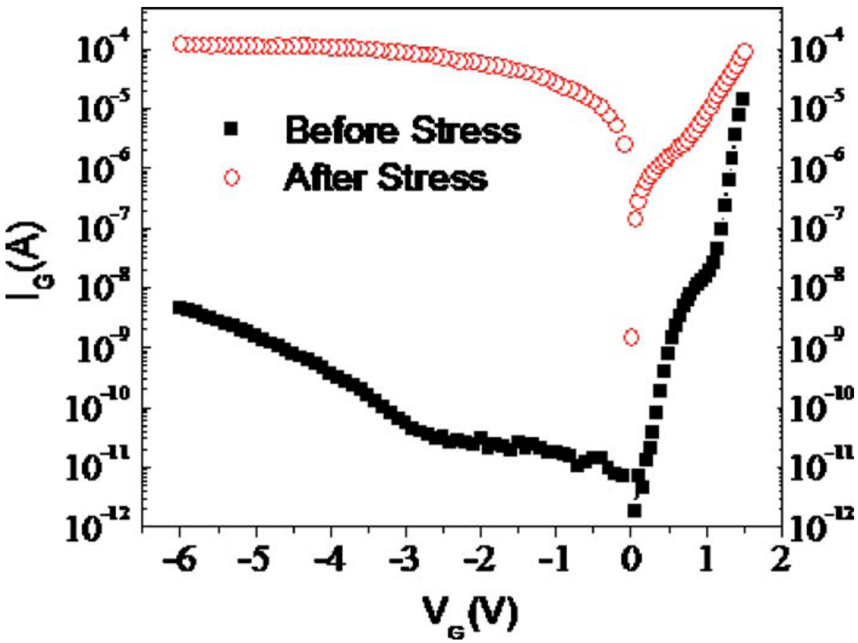
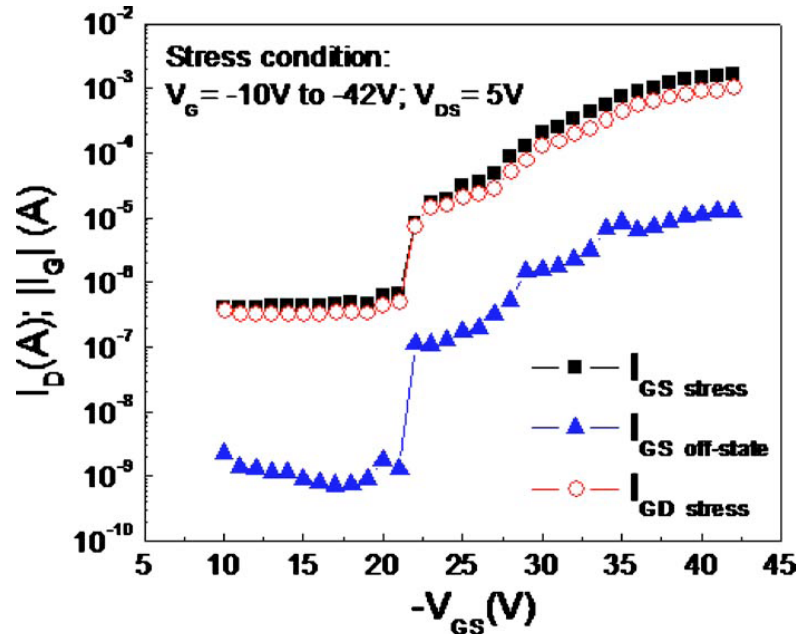
DC Off-State Stress

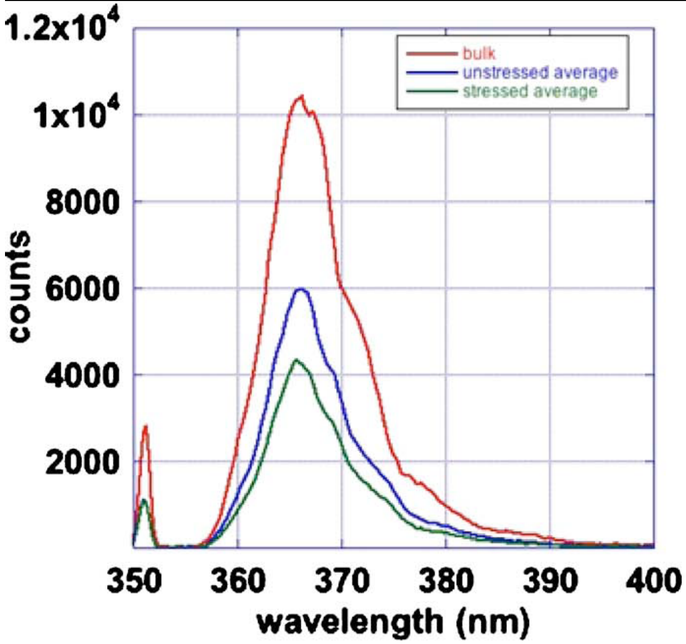




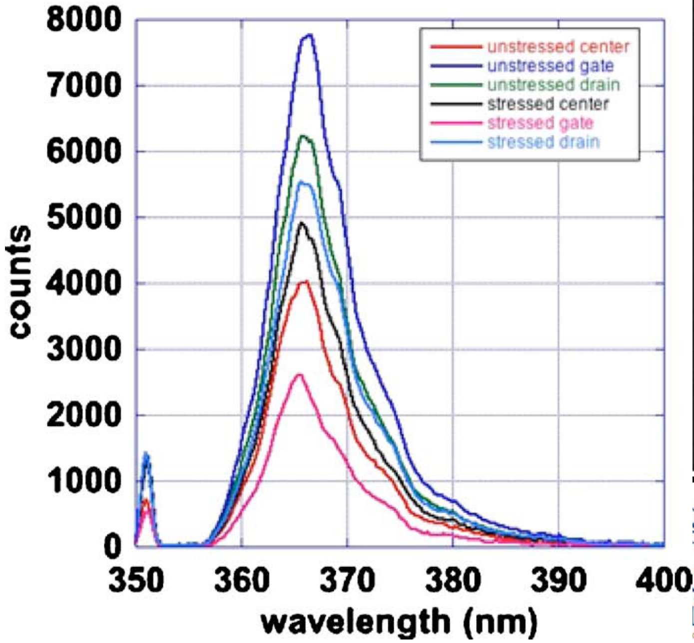
- HEMTs with 0.14 μm gate length step stressed from -10 V to -42 V at -1V/min. V_{DS} = 5V.
- V_{CRI} = -21 V

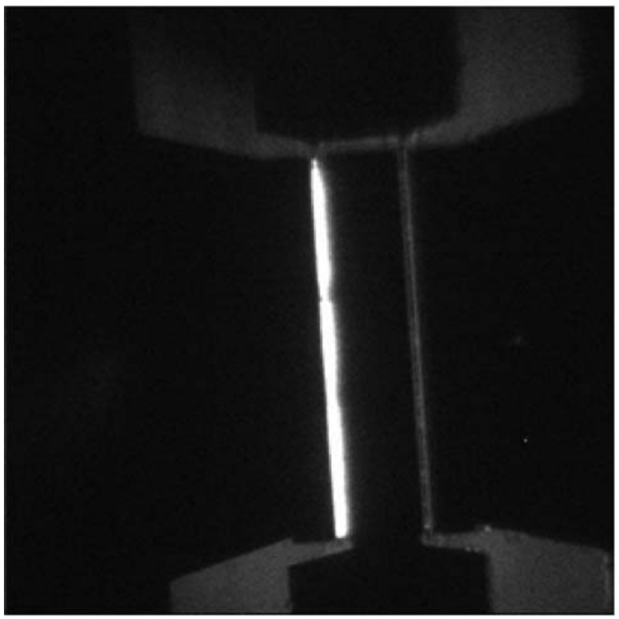
C. Y. Chang, et al. J. Vac. Sci. Technol. B **28**, 1044 (2010).

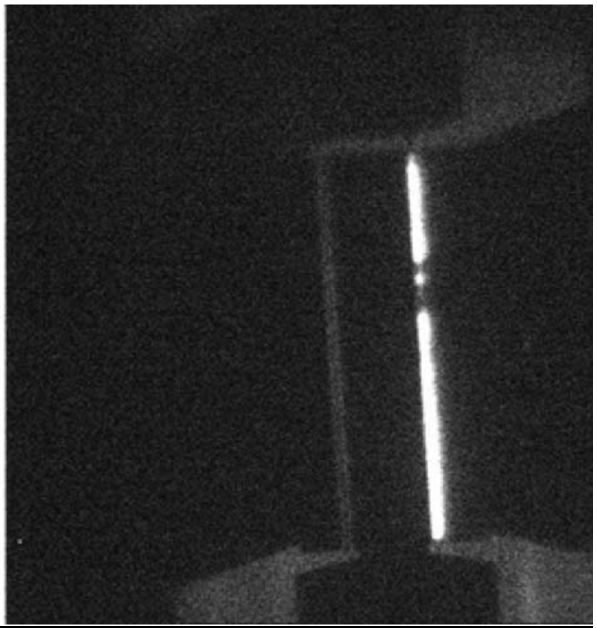
EL & PL



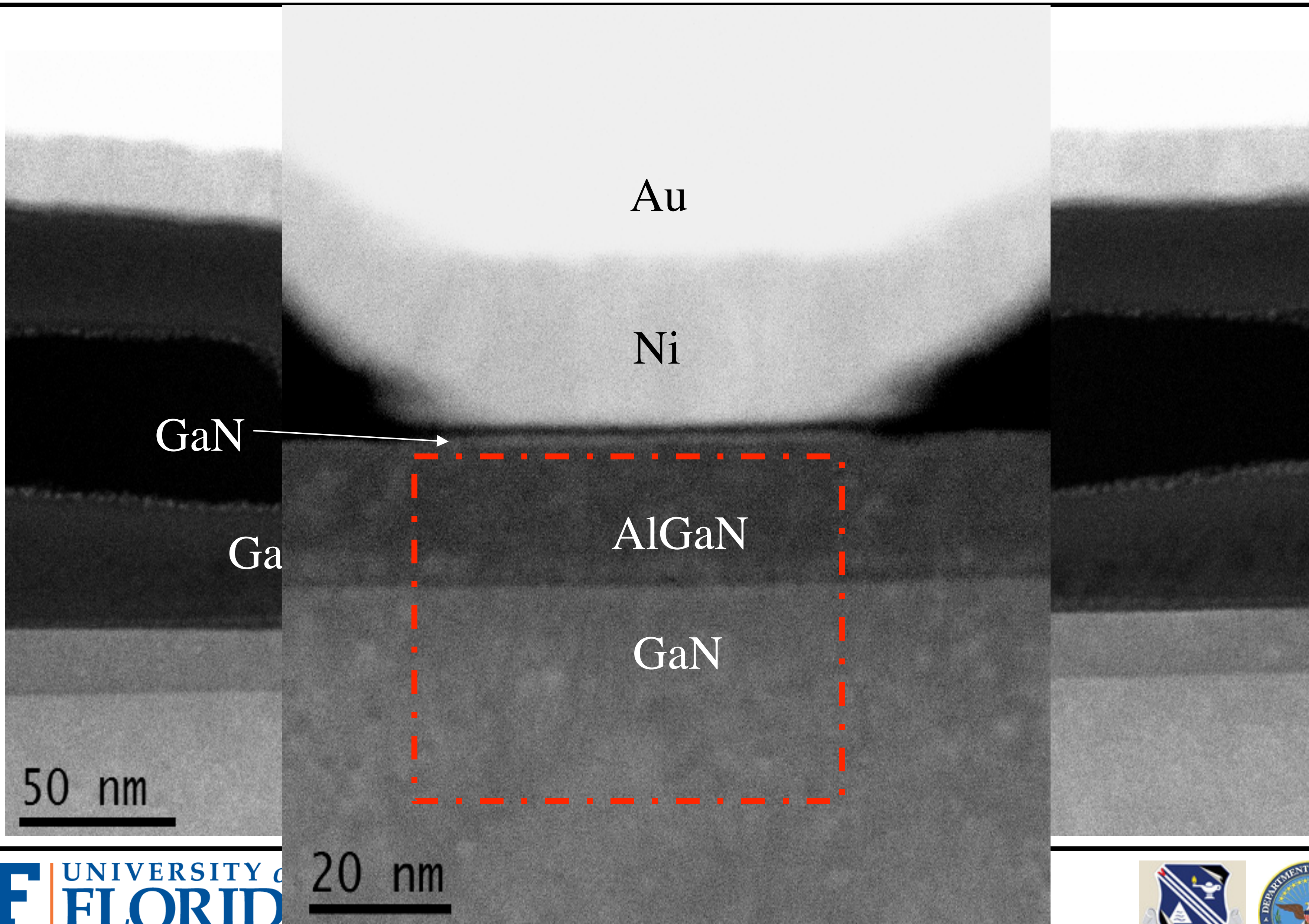
- PL shows non-radiative trap formation increases after stress.
- EL indicates failure may be localized along gate width.



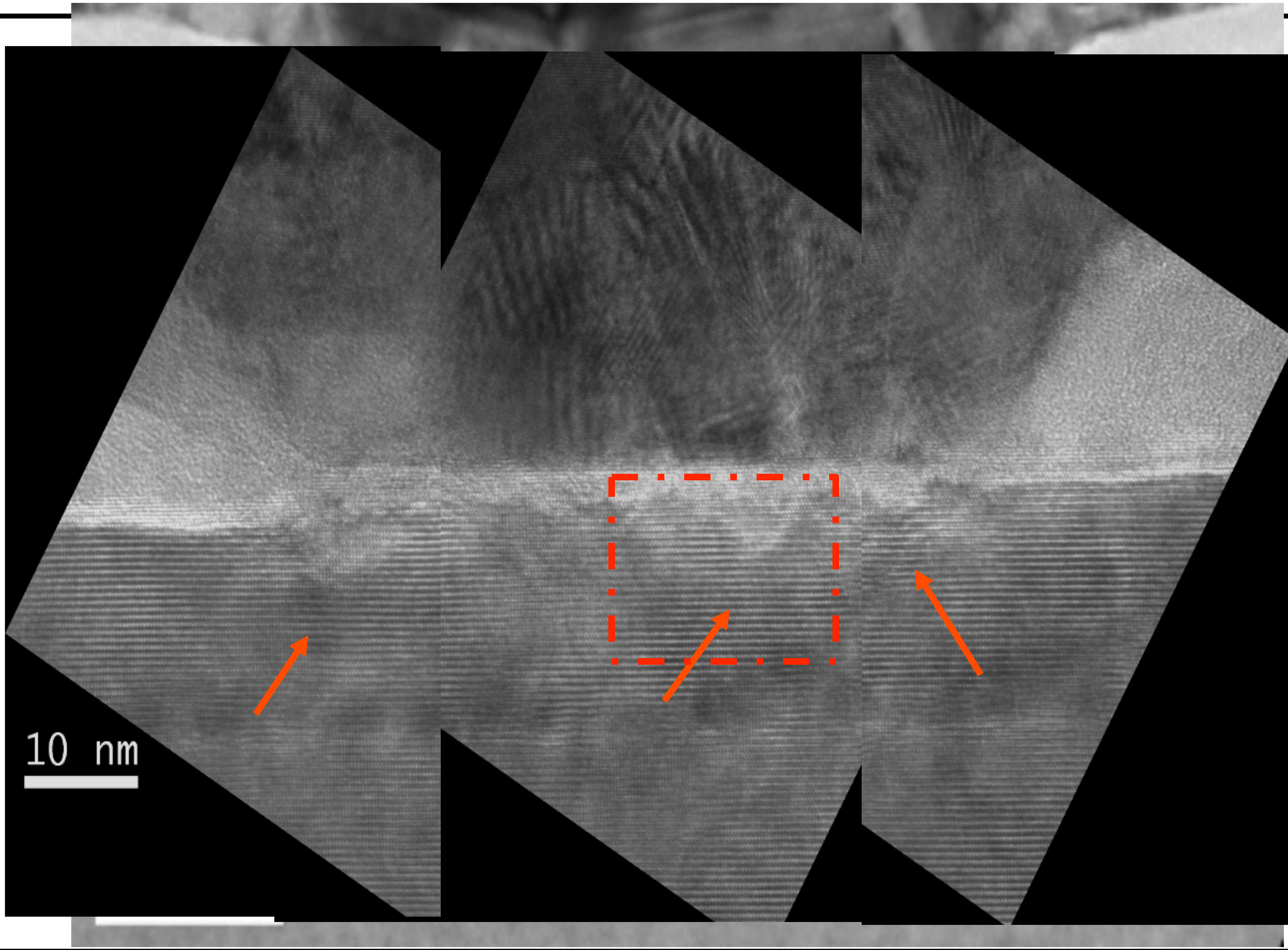




TEM – DC Stress



TEM – DC Stress



Summary of DC Stress

• Off-state stress with varying gate lengths and drain bias conditions indicates **electric field driven degradation**

• EL and PL show increase in non-radiative trap formation after stress

• Degradation likely localized in channel

• Gate metal diffusion, oxide interface intermixing, **absence of crack formation**

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Effect of Off-State Stress on Trap Densities

Numerous studies to understand trapping effects in GaN HEMTs

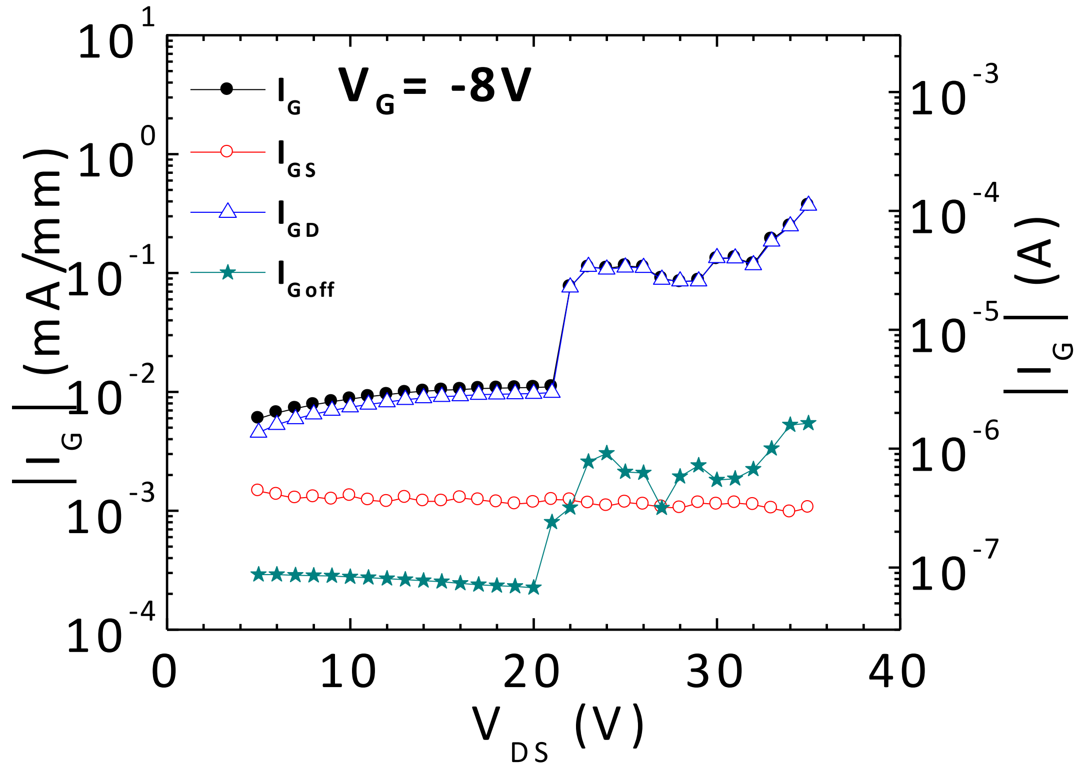
- DLTS — Zhang, et al. J. Electron. Mater. **32**, 388 (2003).
- Conductance DLTS — Gassoumi et al. Physica B **405**, 2337 (2010).
- Transient drain current — Mitrofanov et al. Appl. Phys. Lett. **82**, 4361 (2003).
- Gate leakage current — Tan et al. Appl. Phys. Lett. **80**, 3207 (2002).
- Threshold voltage — Kordos et al. Appl. Phys. Lett. **92**, 152113 (2008).

Investigation of trap states on fresh and off-state stress GaN HEMTs not previously reported

Liu, et al. *Accepted to J. Vac. Sci. Technol. B*

Trap Analysis

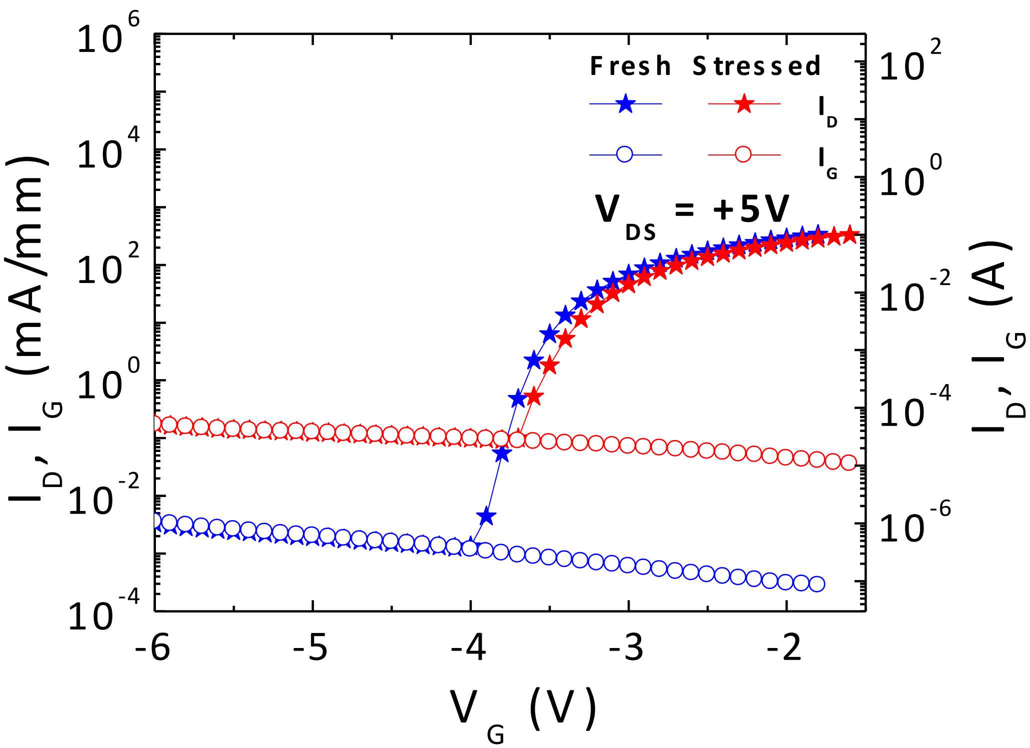
Stress conditions:
V_{GS} = -8V
V_{DS} =5V stepped in
+1V increments



Interface trap density extracted from change in SS with temperature

$$\frac{\partial S}{\partial T} = \frac{k}{q}\ln(10)(1+\varsigma), \varsigma = \frac{C_{it}}{C_{AlGaN}} \qquad D_{it} = {C_{it}}/{q}$$

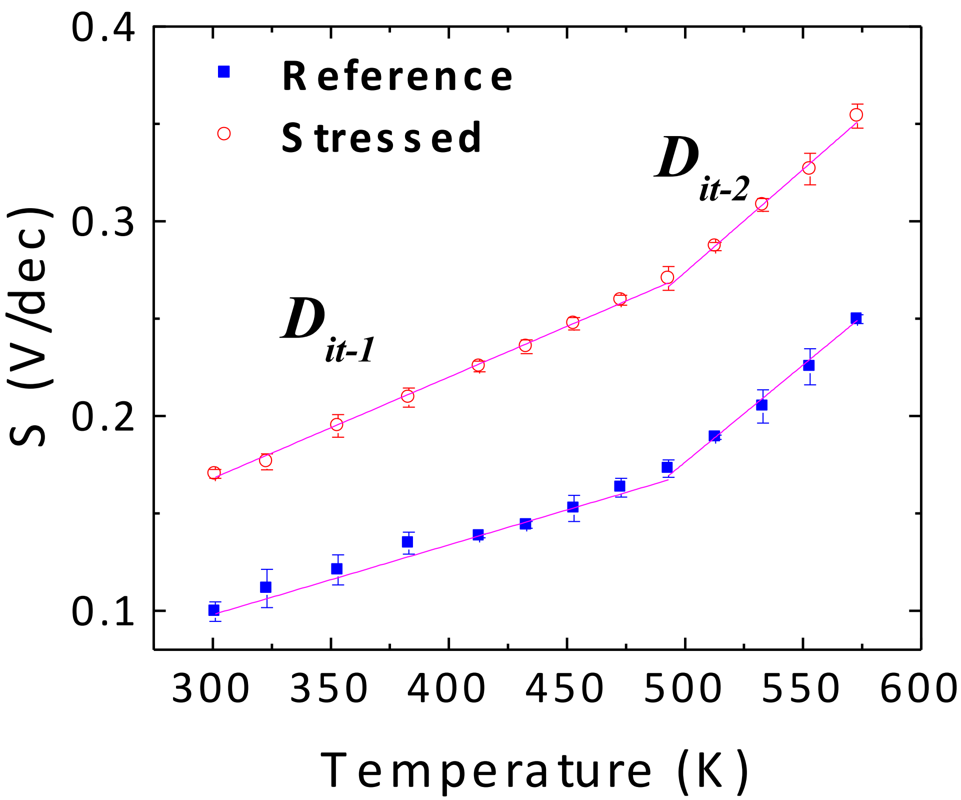
Trap Analysis (2)



Room temperature measurements of fresh and off-state stressed device

Sample	Sub-threshold drain leakage current (μA)	Sub-threshold slope (mV/dec)	ON/OFF ratio
Reference	0.58	98	3.8×10^5
Stressed	37.2	158	5.6×10^3

Trap Analysis (3)

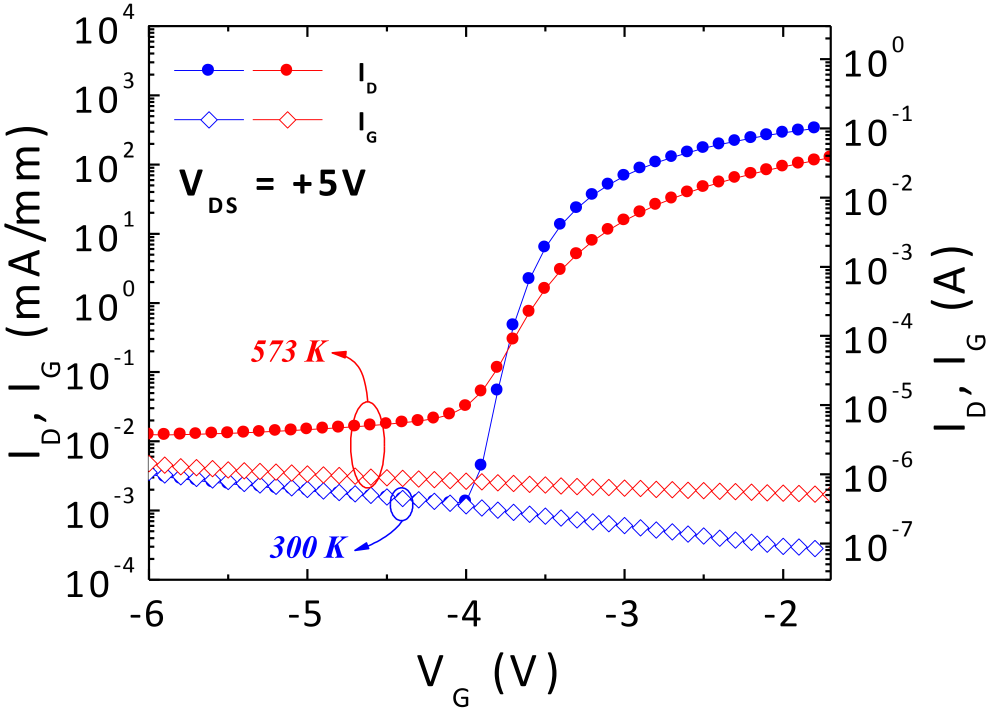


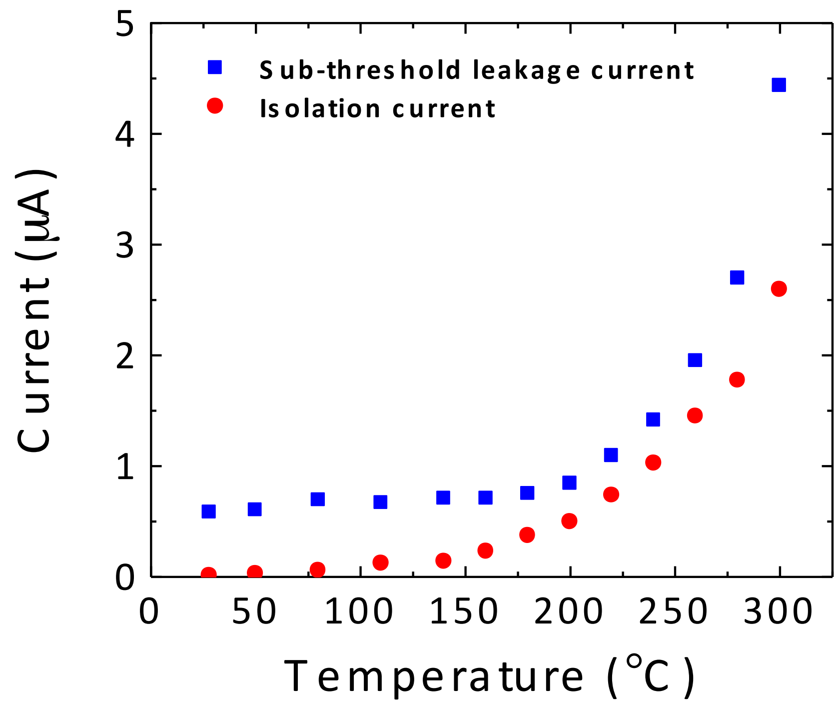
	D_{it-1} ($cm^{-2}V^{-1}$)	D_{it-2} ($cm^{-2}V^{-1}$)
Fresh	1.6 x 10^{12}	8.1 x 10^{12}
Stressed	3.3 x 10^{12}	9.2 x 10^{12}

Increase in trap density after stress due to additional leakage path formations (dislocation generation, gate metal diffusion, etc.)

- Reason for increase from D_{it-1} to D_{it-2}?

Trap Analysis (4)

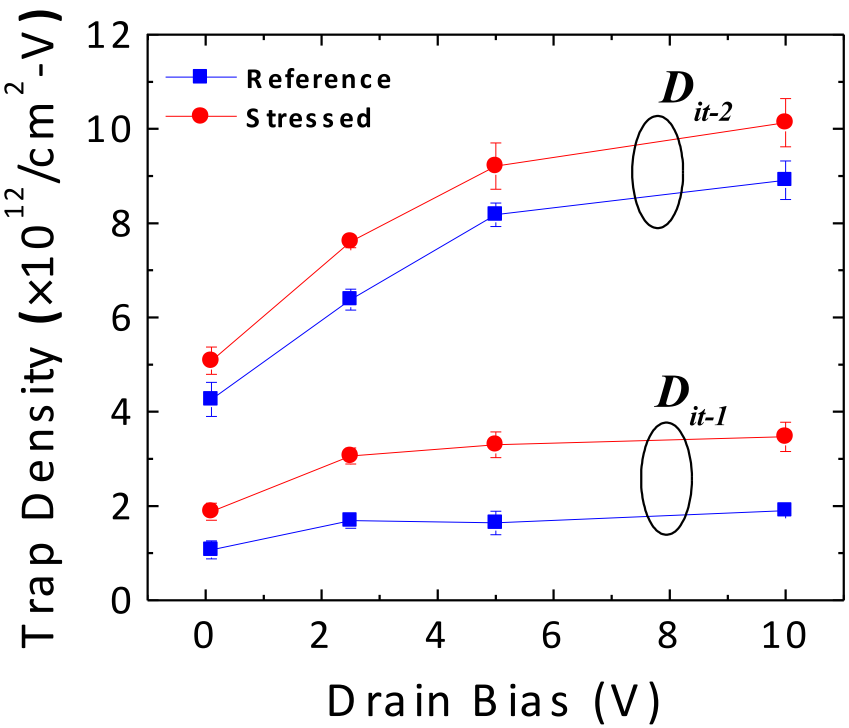


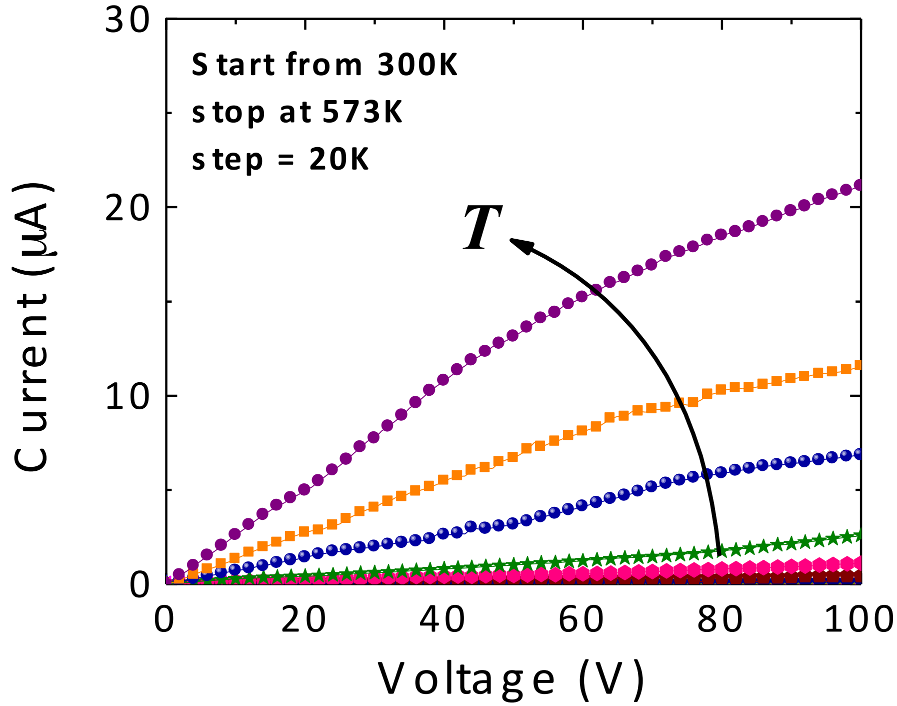


@ R.T. : Drain leakage current = gate leakage current

@ 573 K: Drain leakage current ≠ gate leakage current

Trap Analysis (5)





D_{it-1} less sensitive to drain bias voltage than D_{it-2}

Summary of Trap Density

- At low temperatures, trap density increased ***> 2X*** due to off-state stress.
- Above 493 K, device isolation currents dominated leakage currents of device (D_{it-2})
- Traps thermally activated due to deep traps induced by ion bombardment from ICP

  (Thermal anneal or ion implantation for isolation)
- Traps created during stress and those activated at high temperature played role in increase of trap densities.

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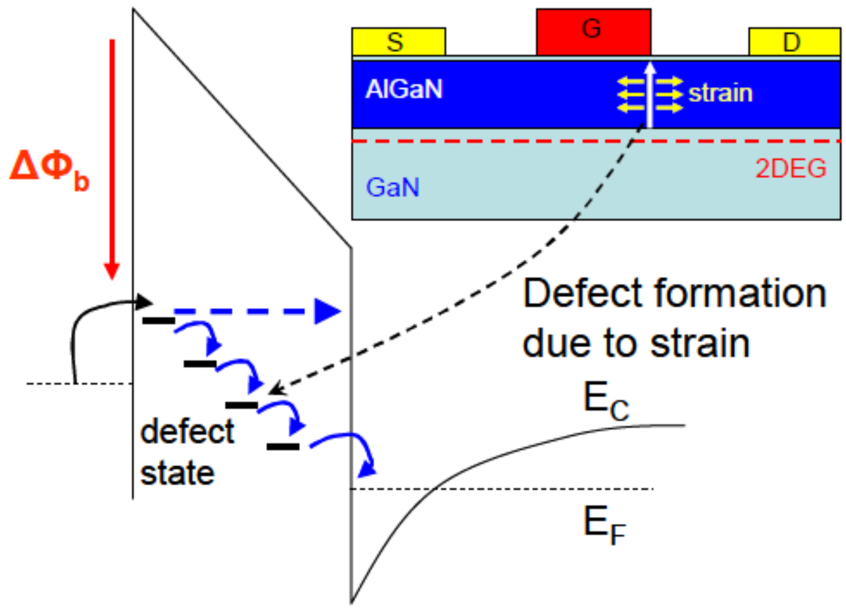
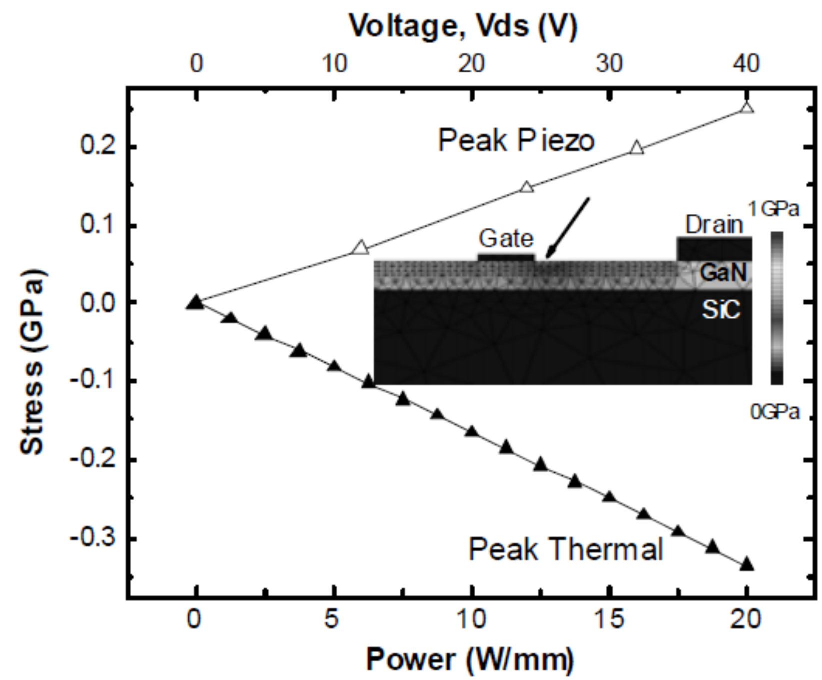
Temperature Dependence V_{CRI}

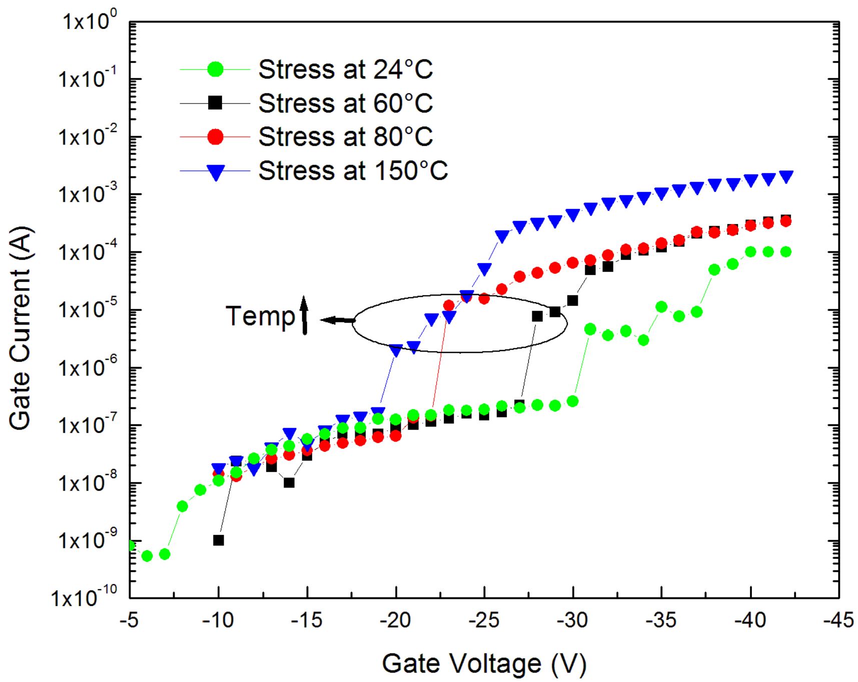


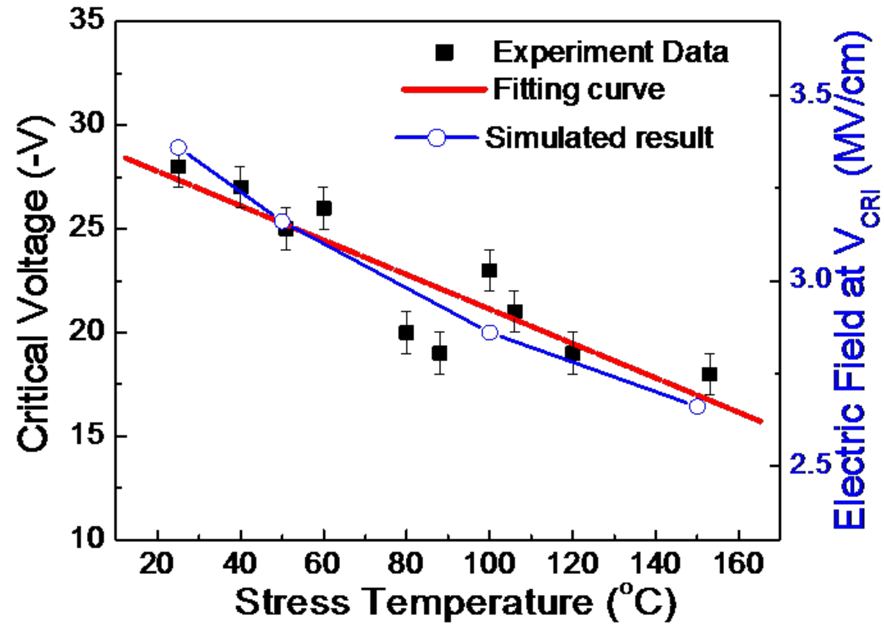


J. A. del Alamo, J. Joh. Microelectronics Reliability, 49 (2009) 1200–1206.

A. Sarua, et al. Proc. CS Mantech Conf. 8.5 (2009).

Temperature Dependence V_{CRI} (2)



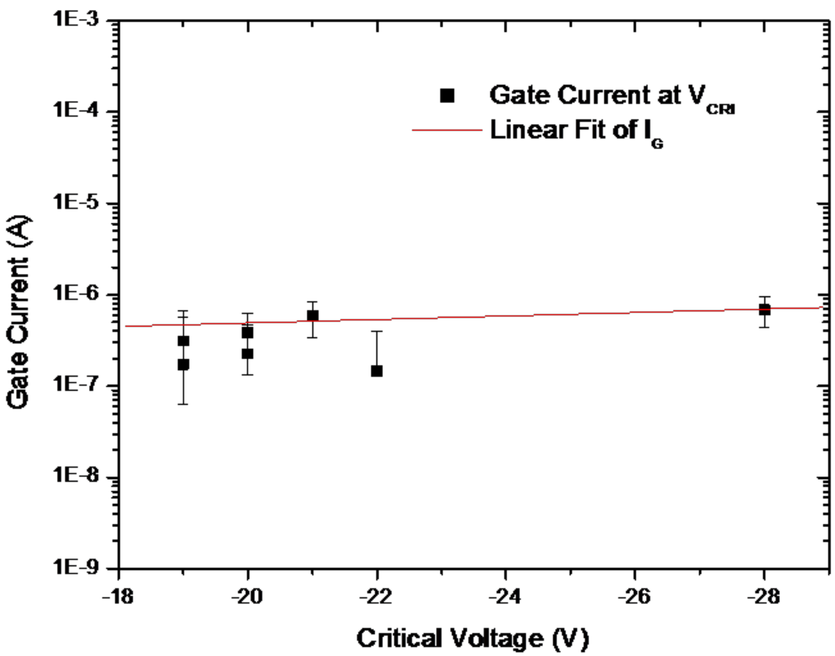


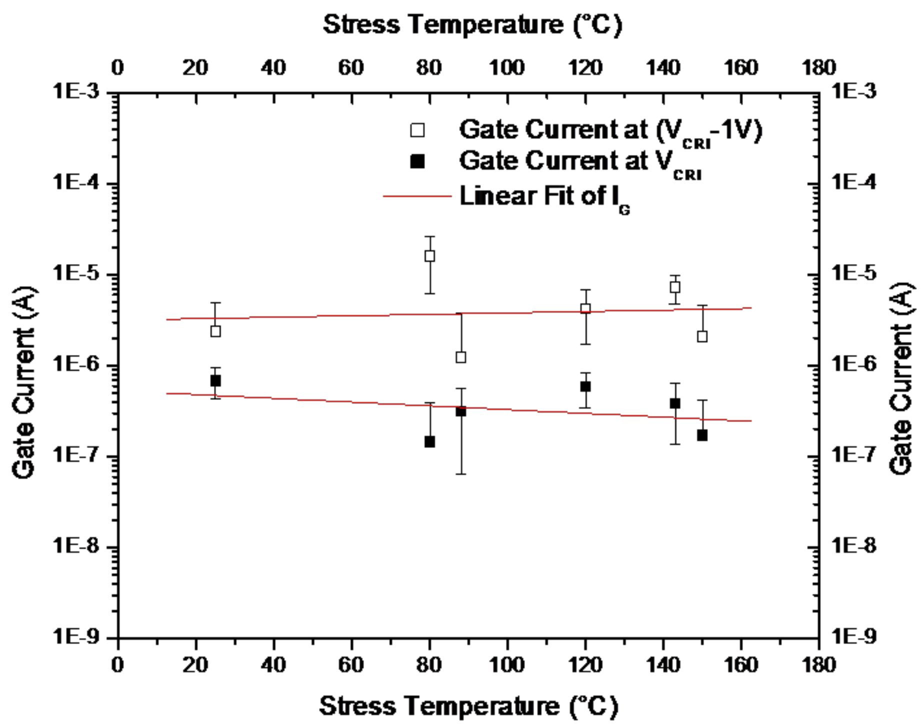
- Critical voltage decreases with increasing temperature.
- Linear dependence observed.

E. A. Douglas, et al., *Microelectron Rel, in press*

Temperature Dependence V_{CRI} (3)

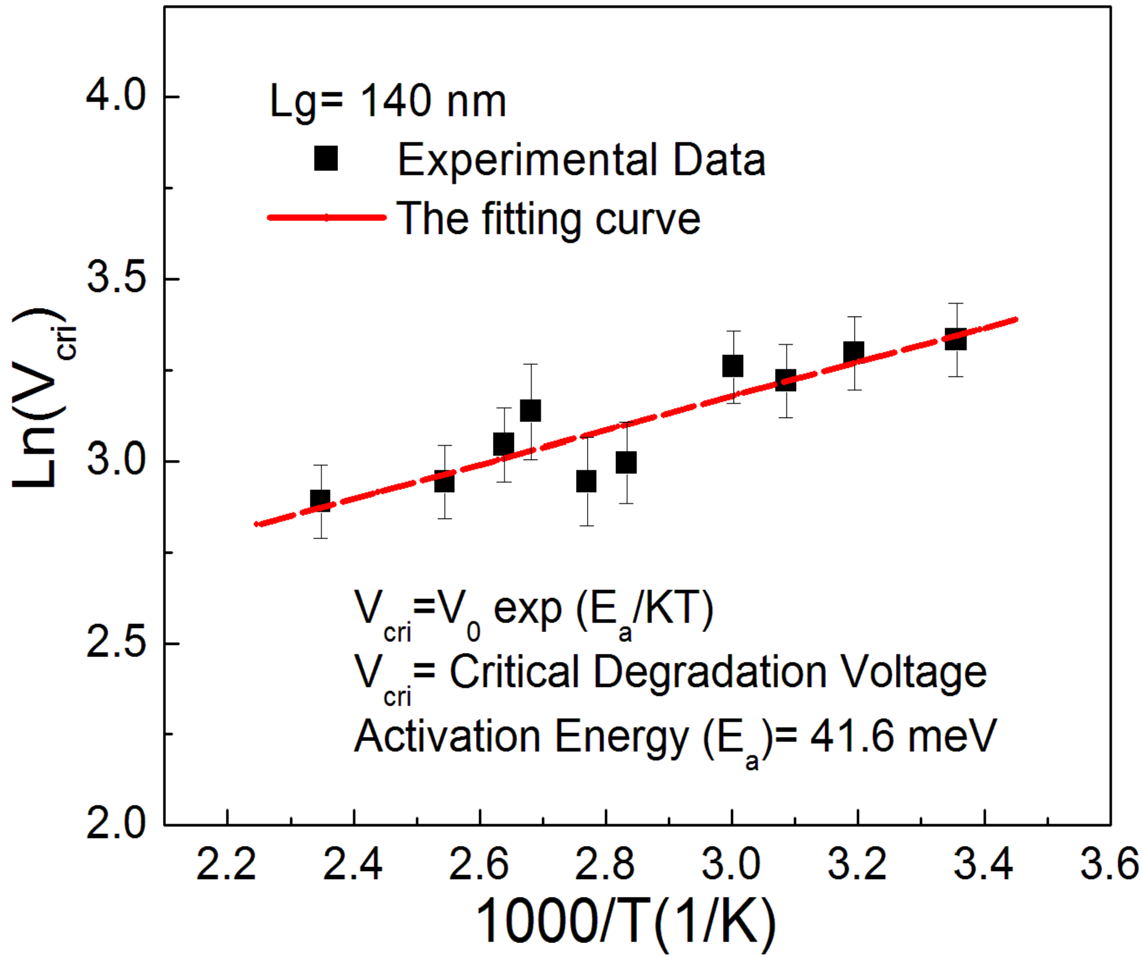
- Gate leakage current similar, independent of critical voltage.
- Current similar **at** and immediately **after** V_{CRI}

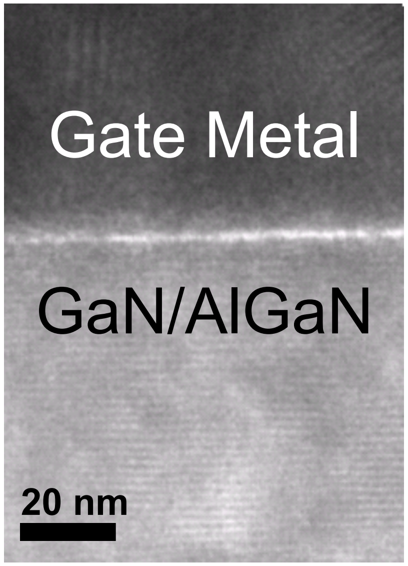


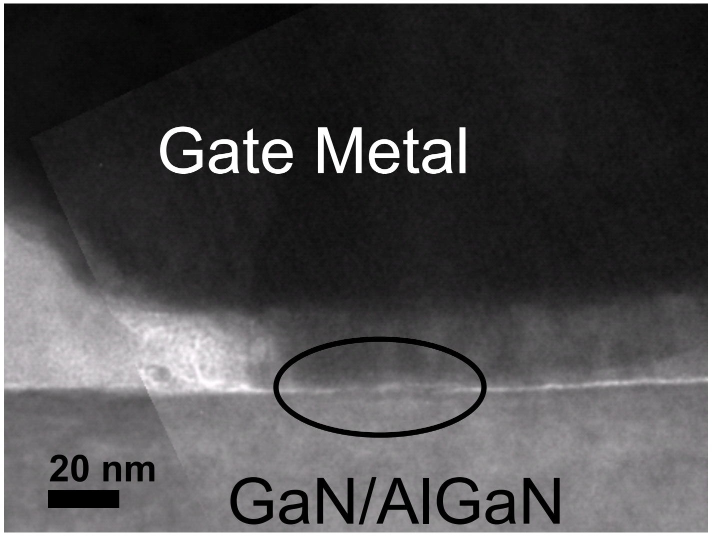


Temperature Dependence V_{CRI} (4)

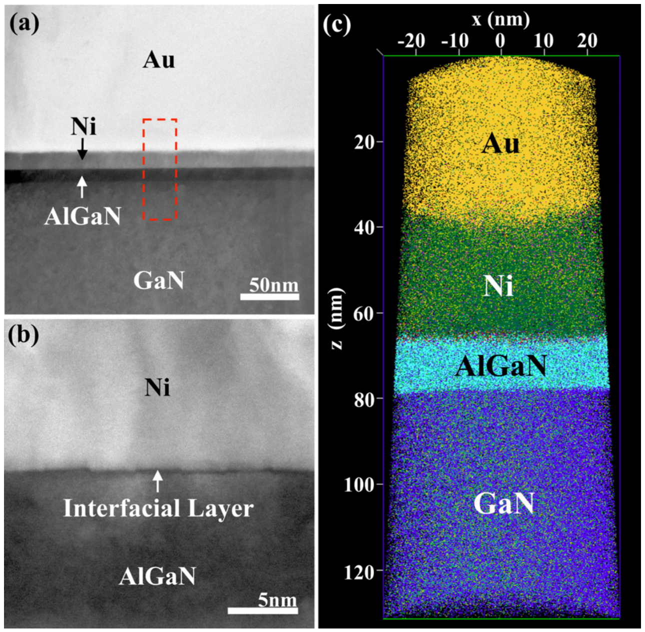
- Small activation energy: 41.6 meV

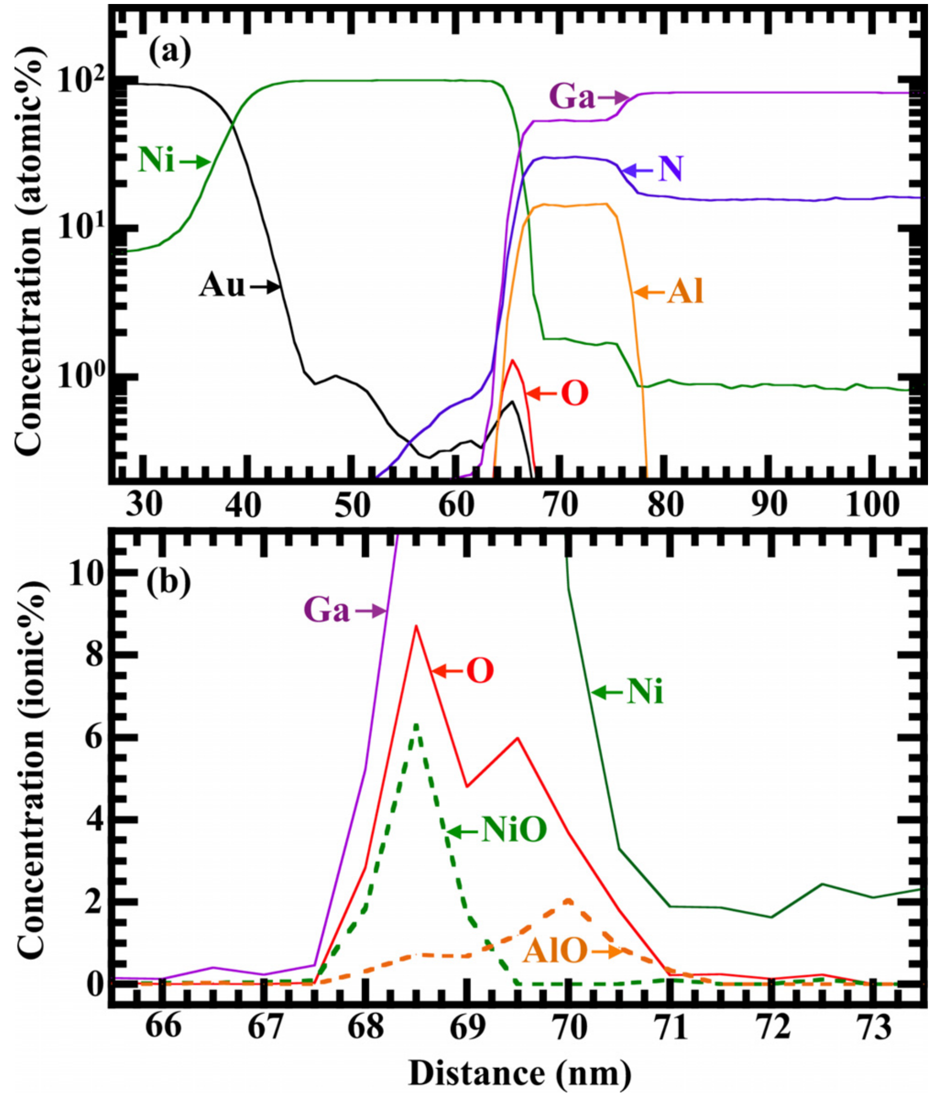






LEAP Analysis - Commercial Sample





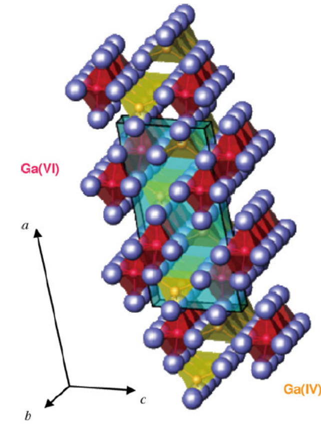
- 2-D concentration profiles of Au, Ni, O, Ga, N, and Al
- 40 nm data pipe orthogonal to interface
- Abrupt interface between NiO and AlO

M. R. Holzworth, *et al*., *Appl*. *Phys*. *Lett*. 98, 122103 (2011).

TDDB

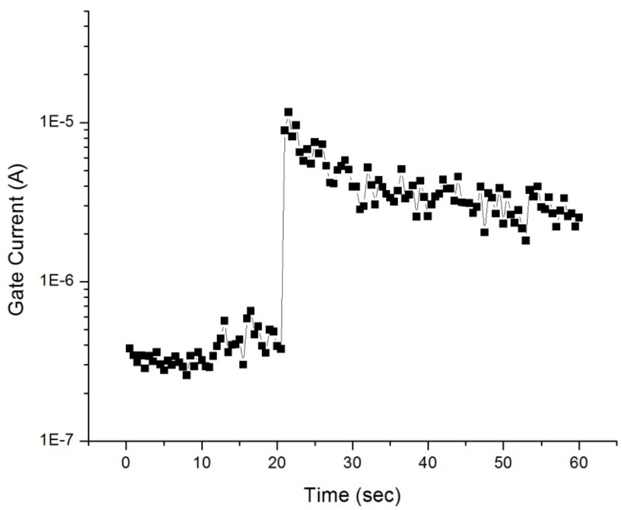
➢ Presence of interfacial oxide layer due to processing/fabrication

➢ Oxide layer can provide additional mechanism for degradation



β- Ga_2O_3 lattice

H. Hosono, *Handbook of Transparent Conductors*, Springer, 2010.



Ga-O bond is ~60% ionic, leading to a **very polar bond**, susceptible to bond distortion under electric field.

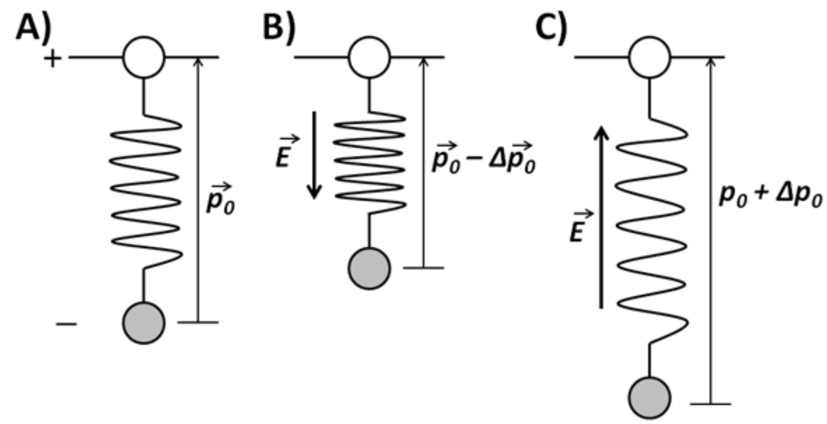
TDDB (2)

Using thermochemical electric field model for TDDB in thin SiO_2

J. W. McPherson, H.C. Mogul, J. Appl. Phys. **84**, 1513 (1998).

Applying model to Ga_2O_3

$$\boldsymbol{E}_{loc} = \boldsymbol{E}_{ox} + L(\boldsymbol{P}/\epsilon_0) \qquad \boldsymbol{P} = \chi\epsilon_0\boldsymbol{E}_{ox}$$



Total polarizability (ionic & electronic component)

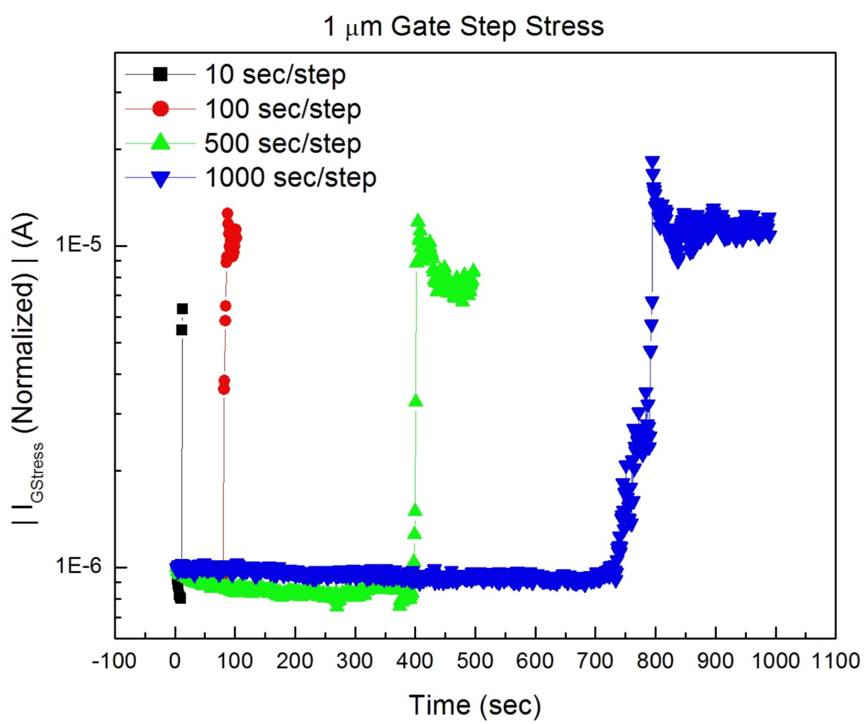
$$\alpha^t = \frac{3(\epsilon_r - 1)\epsilon_0}{(\epsilon_r + 2)N_V}$$

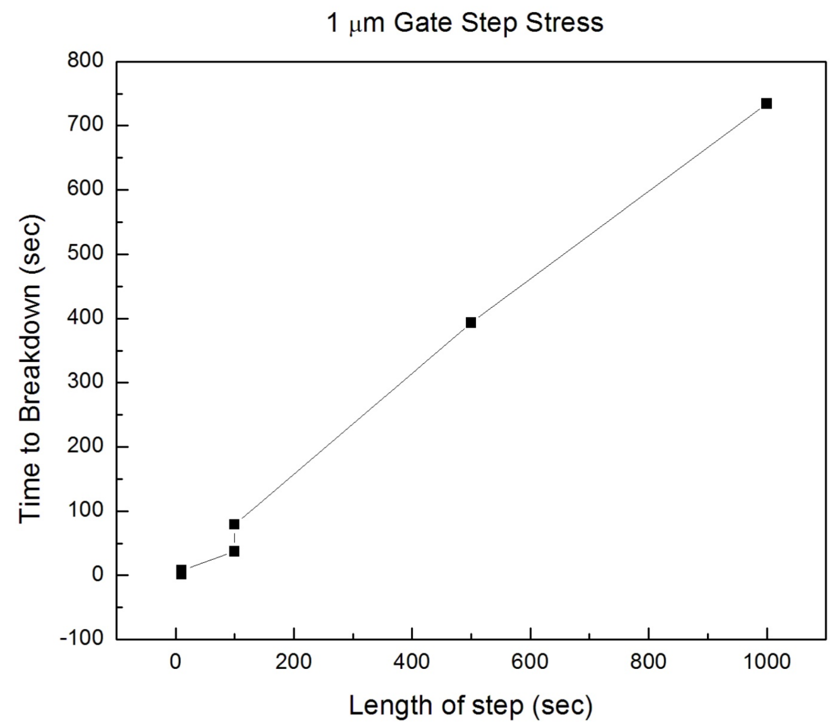
Bond distortion due to ionic component of induced molecular dipole moment

$$\Delta x = \frac{\alpha^{(t)}(\chi + 3)E_{ox}}{15(Z^*e)\cos(\theta)}$$

~10.5% displacement at 2 MV/cm for Ga_2O_3 resulting in anharmonic coupling to lattice

TDDB (3)





As time step interval is increased, time to breakdown increases, with observed linear dependence on step length.

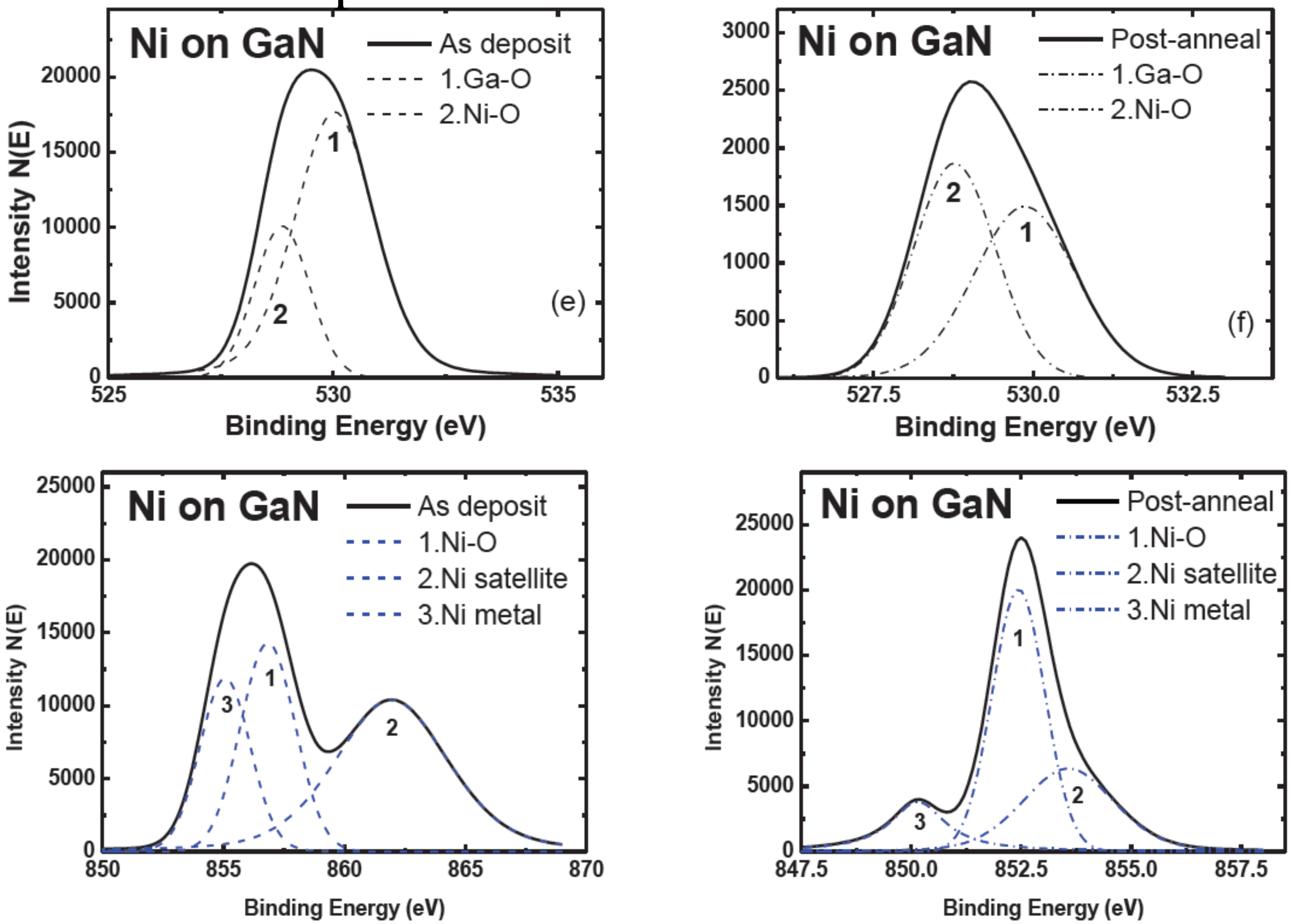
➢ Amit Gupta from Dr. Nishida's group to discuss additional results

X-ray Photoelectron Spectroscopy

As-deposited | Post-anneal

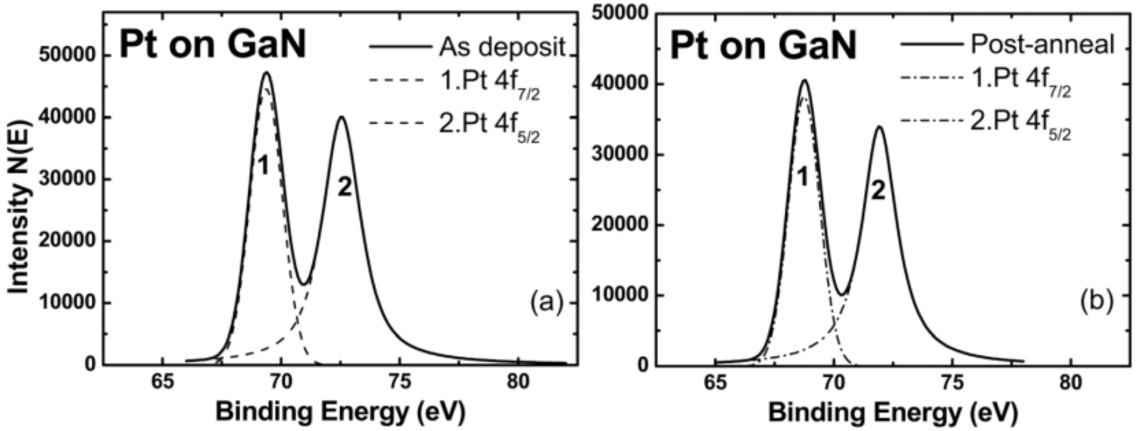
O 1s

Ni 2p

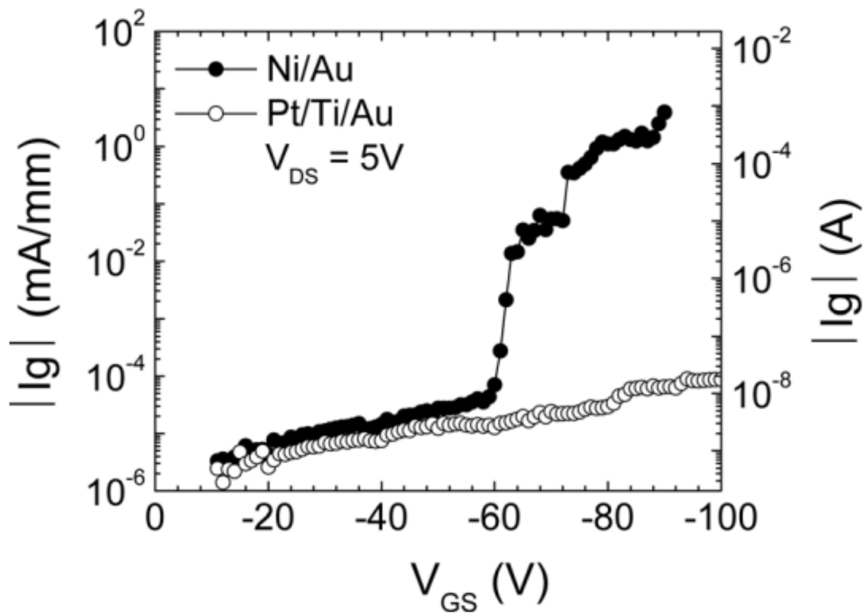


Lu Liu, *et al*., J. Vac. Sci. Technol. B 29, 042202 (2011). C. F. Lo, *et al*., Electrochem. Solid-State Lett. 14, H264 (2011).

Pt Gate



Pt on GaN
As deposit
1.Pt 4f7/2
2.Pt 4f5/2
Intensity N(E)
Binding Energy (eV)
(a)
Pt on GaN
Post-anneal
1.Pt 4f7/2
2.Pt 4f5/2
Binding Energy (eV)
(b)



Ni/Au
Pt/Ti/Au
VDS = 5V
|Ig| (mA/mm)
|Ig| (A)
VGS (V)

Summary – Temperature Dependence

- Decrease of V_{CRI} with **increase** in temperature, not expected if due only to stresses in device
- Presence of oxide layer, and consumption of interface after stress, indicates degradation through oxide breakdown creating leakage path
- Breakdown strongly dependent on step stress time interval.
- XPS indicates that Ni is highly reactive in the presence of oxygen, particularly at elevated temperatures.

Overview

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C. Effect of Temperature

III. RF Stress Results

A. Drain Bias Dependence

B. Photoemission

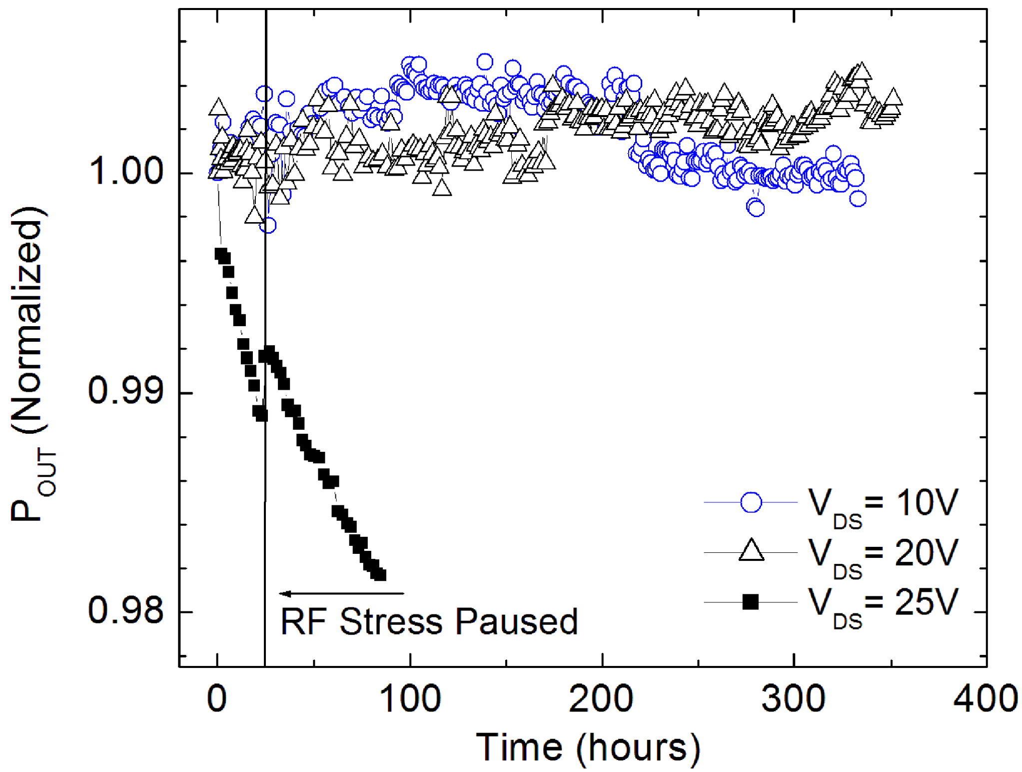
IV. Conclusion

Stress Conditions (RF)

- Stressed at AFRL on AccelRF system
- 0.125 μm gate length, 10 GHz stress at 3 dB and 3.7 dB compression point
- Class AB condition, I_{DQ} = 200mA/mm
- Baseplate temperature from 30 – 120°C

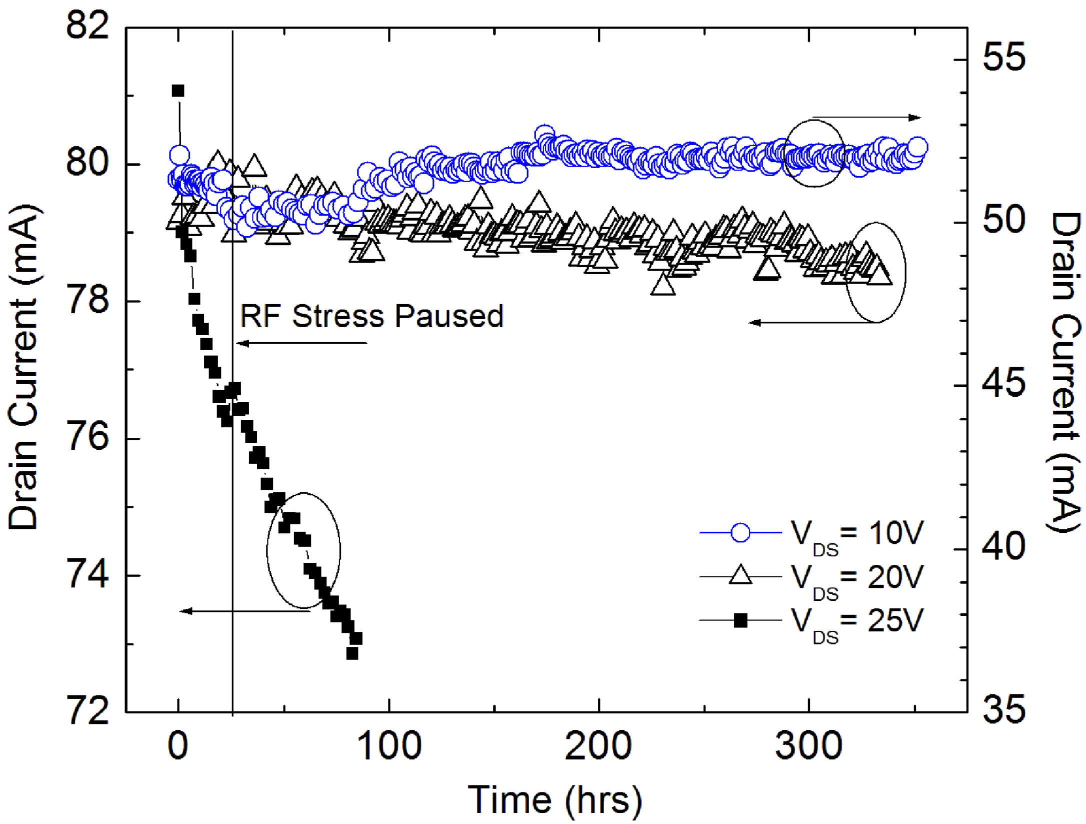
RF Stress – Drain Bias

- Devices stressed at V_{DS} = 10, 20, 25, 30 V
- Up to 350 hours RF stress
- Temperature = 30C



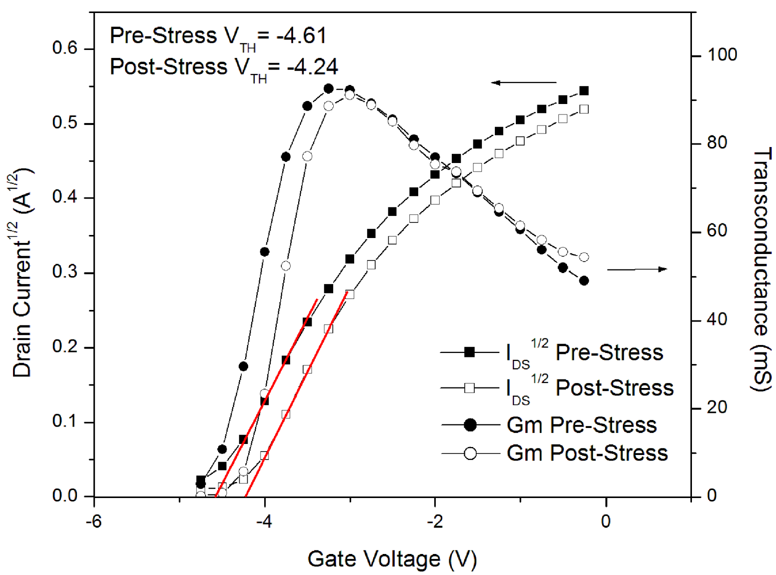
E. A. Douglas, *et al.*, *Electrochemical Solid-State Letters*, **14** (11) H464-H466 (2011).

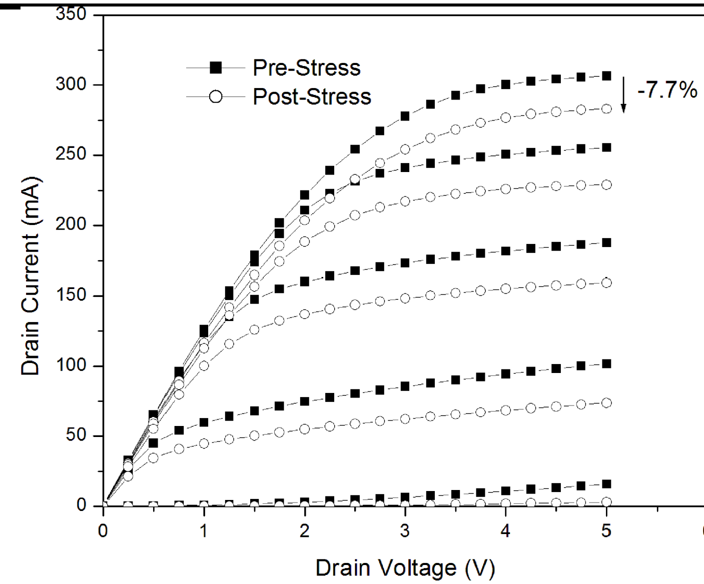
RF Stress – Drain Bias (2)



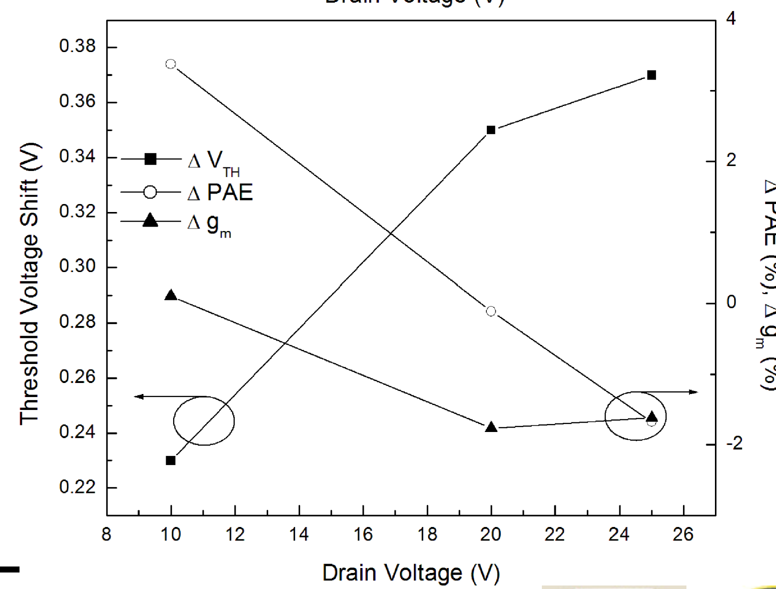
- Apparent burn-in at 10 V
- Dissipated power at 20V and 25V are 3.5 W/mm and 3.77 W/mm
- ΔR_{TH} ~1.5%, within error
- V_{CRI} for this device ~ -23V

RF Stress – Drain Bias (2)



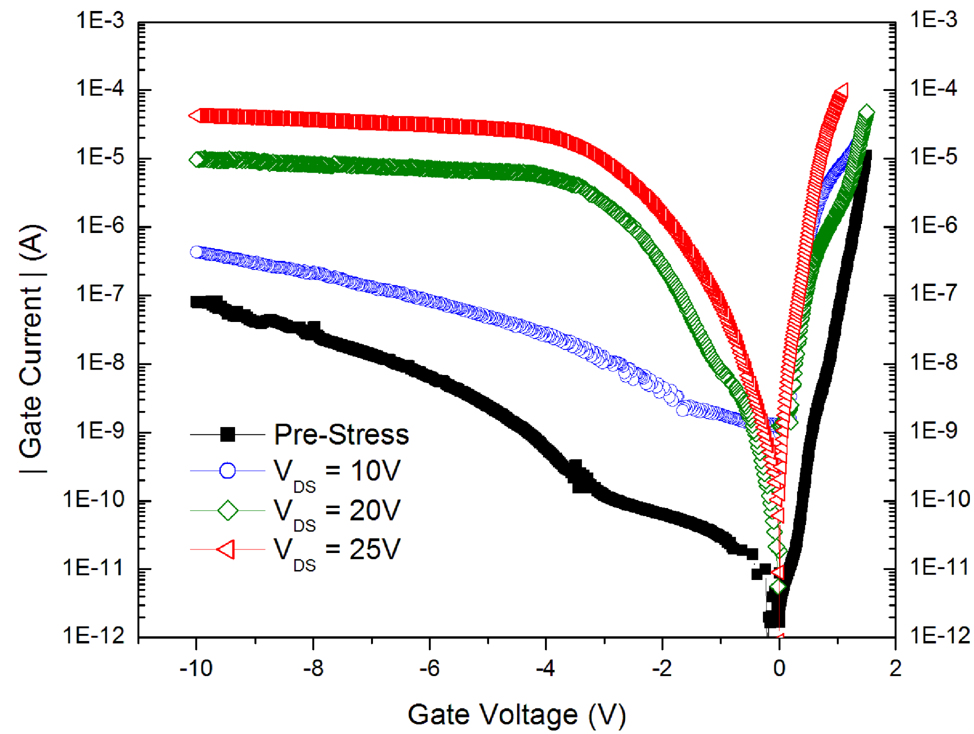


- I_{DSS}, g_m, PAE, and gain show minimal degradation.
- Large shifts in V_{TH}



RF Stress – Drain Bias (3)

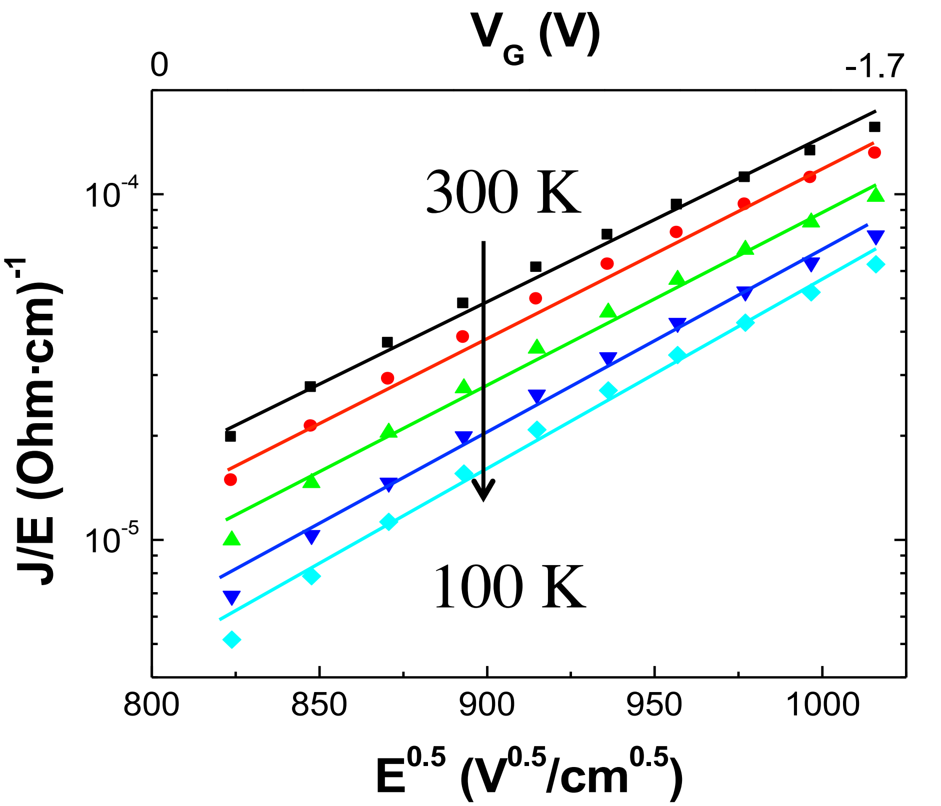
- Gate leakage current increases several orders of magnitude.
- Schottky barrier height decreases from 673 mV to 602 mV
- Schottky contact likely point of degradation
- $E_A = 0.45$ eV



Characterizing Trap Levels

Measured E_{AlGaN} used to understand tunneling mechanism

Poole-Frenkel dominant at low field



Poole-Frenkel Model:

$$J = CE_{AlGaN} \exp\left[-\frac{q\left(\phi_t - \sqrt{qE_{AlGaN}/\pi\varepsilon_0\varepsilon_s}\right)}{kT}\right]$$

$$\equiv m(T)\sqrt{E_{AlGaN}} + b(T)$$

Can estimate trap level using E_{AlGaN}

AFRL SiC: $\phi_t = 0.46 \pm 0.01\text{eV}$

Nitronex: $\phi_t = 0.11 \pm 0.09\text{eV}$

*extracted at 250 and 300 K

Nishida's group, MURI Review, May 2011

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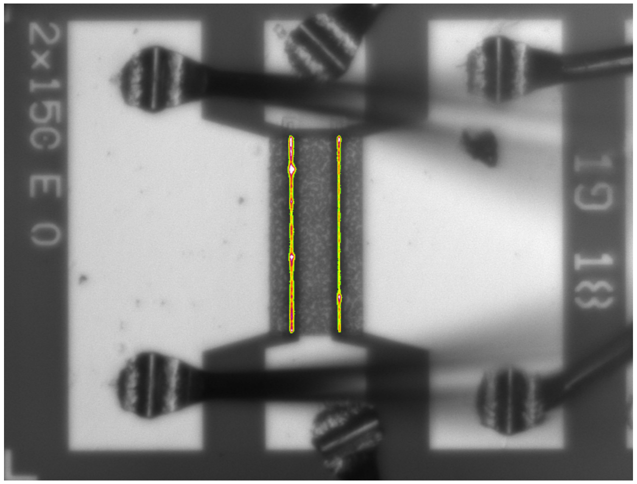
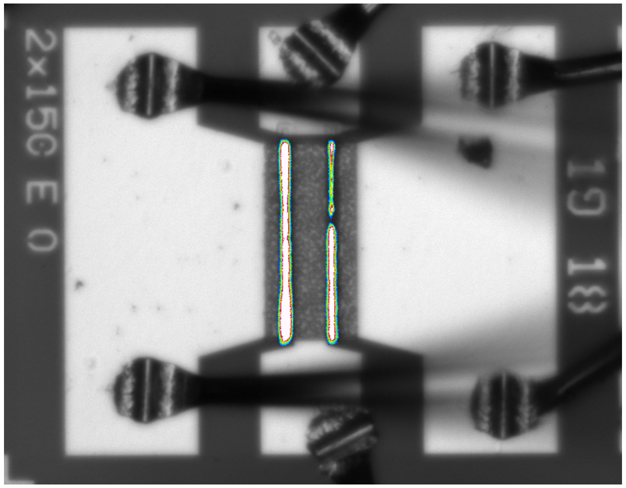
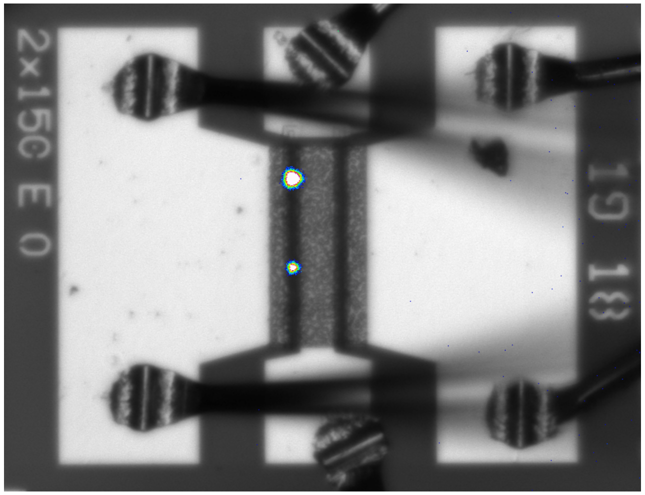
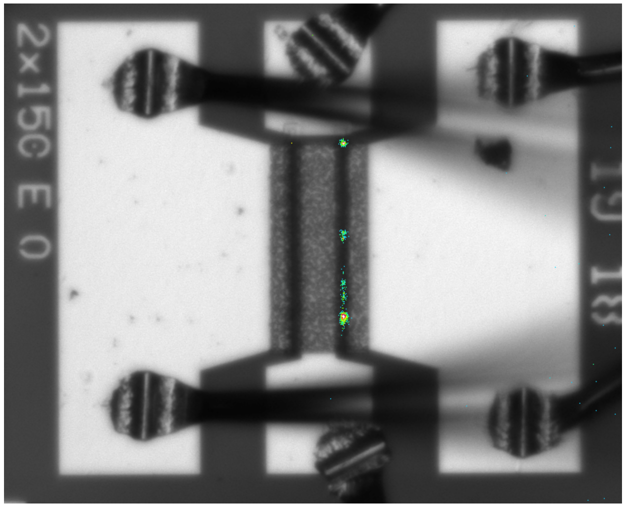
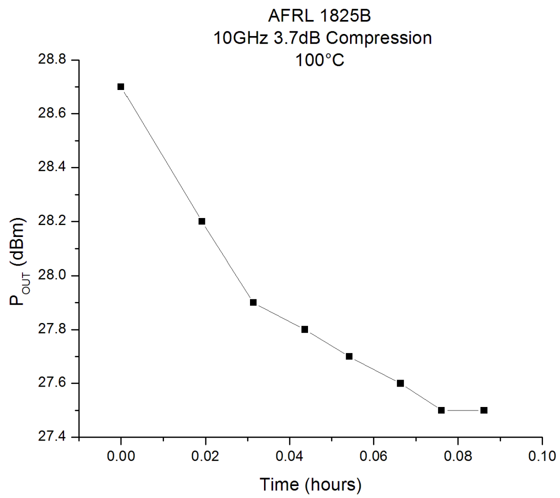
Photoemission

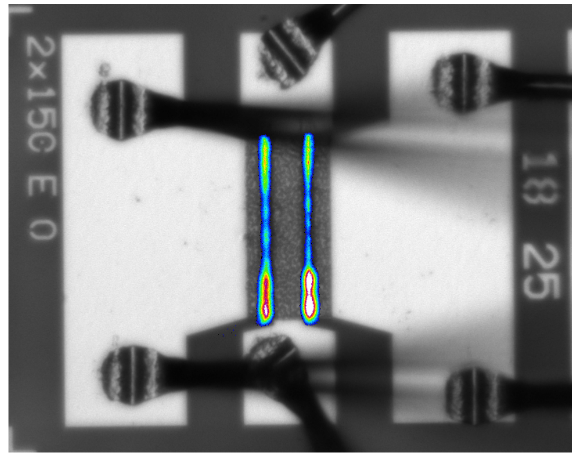
	Pre-Stress	Post-Stress
Forward Bias (I_{DS} = 50mA)		
Reverse Bias (V_{GS} = -10V)		

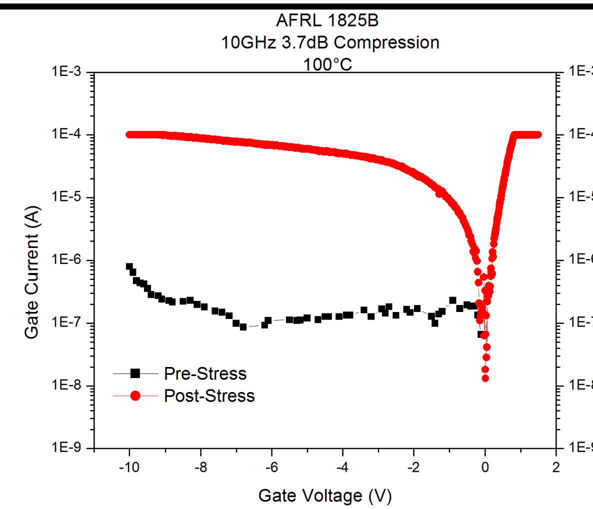
Douglas, et al. *CSICS, 2011 IEEE* , vol., no., pp.1-4, 16-19 Oct. 2011

Photoemission - Screening

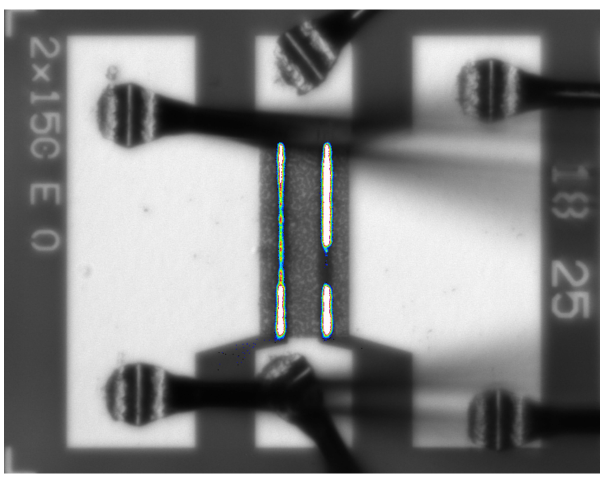


Forward Bias

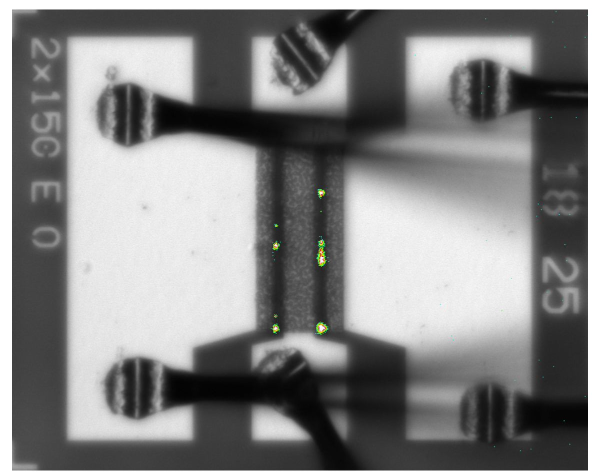




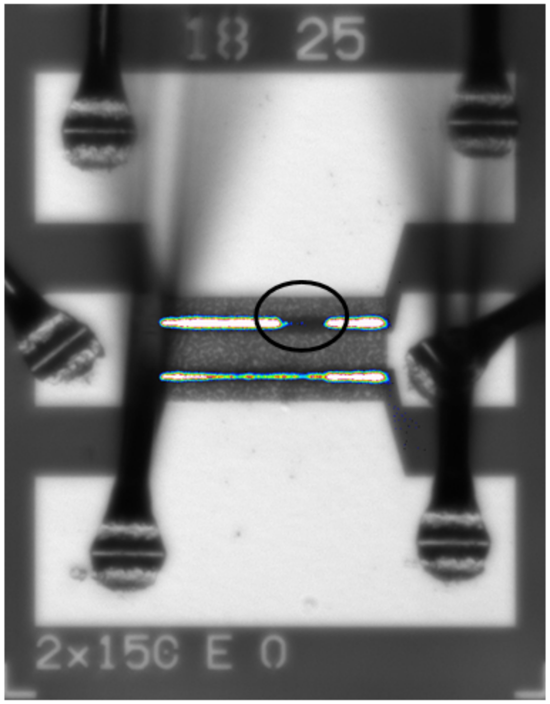
Forward Bias

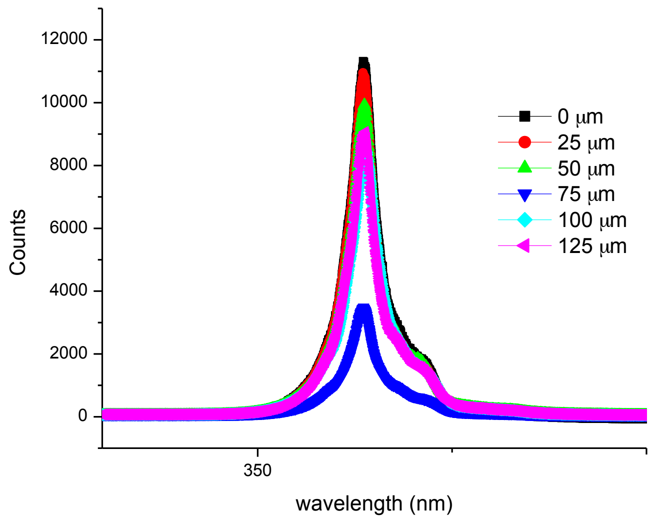


Reverse Bias

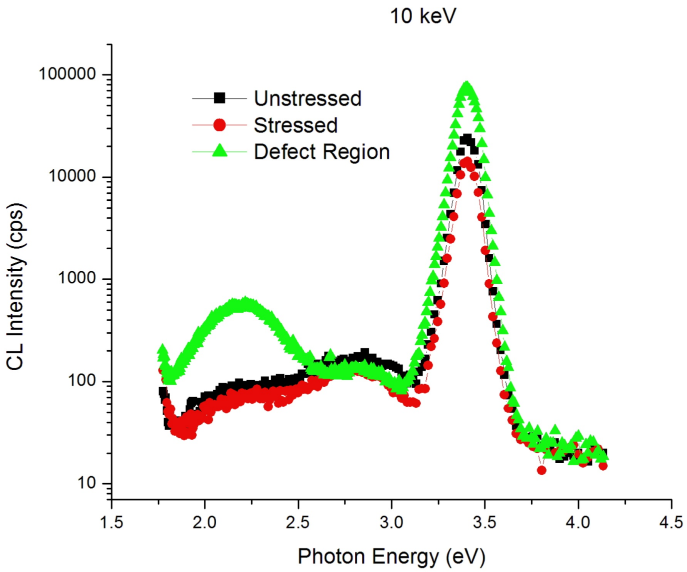


Photoemission and μ-PL





➢ Brent Gila to discuss additional results



- μ-PL confirms increase in non-radiative trap formation
- CL indicates increase in YL emission in defective region

Summary – RF Stress

- RF and (most) DC device characteristics show stability up to drain bias of 20V.
- Slight increase in P_{OUT} at V_{DS} =10V, but all three drain bias conditions show increase in I_{GS} , indicating gate degradation.
- EL recombination sites not similar after stress
- Non-uniform EL only precursor for infant mortality in device
- Activation energy similar to Dr. Nishida's group (~0.45 eV)

Conclusion

DC STRESS

- Off-state stress with varying gate length and drain bias shows electric field driven degradation
- Off-state stress results in increase of non-radiative trap formation (EL & PL), may be localized along gate width.
- Two trap densities present pre- and post- off state stress, deep traps due to ICP etching activated at high temperature.
- Drain bias dependence observed with D_{it-2}.
- Negative temperature dependence with V_{CRI}, E_A= 42 meV.
- Degradation due to breakdown of oxide interface

RF STRESS

- RF stress shows threshold drain bias. Similar to V_{CRI}.
- Schottky contact degradation observed at all drain bias
- E_A = 0.45 eV (also reported by Dr. Nishida's group)
- EL / CL / PL indicates higher defects localized along channel after stress